

LH-22S83D SERVICE MANUAL

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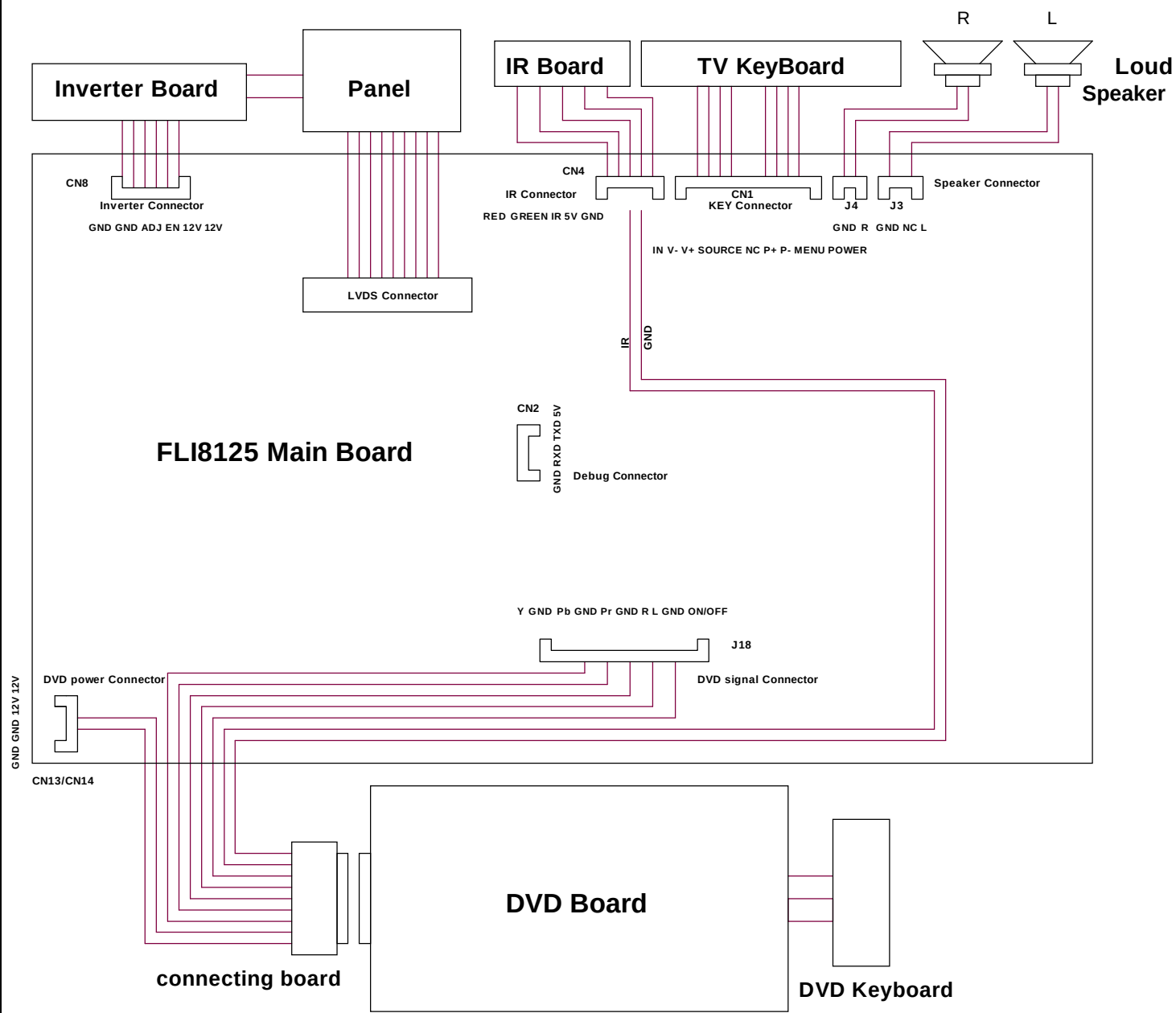
PART 4: Detailed Circuit

- ◆ Main Board
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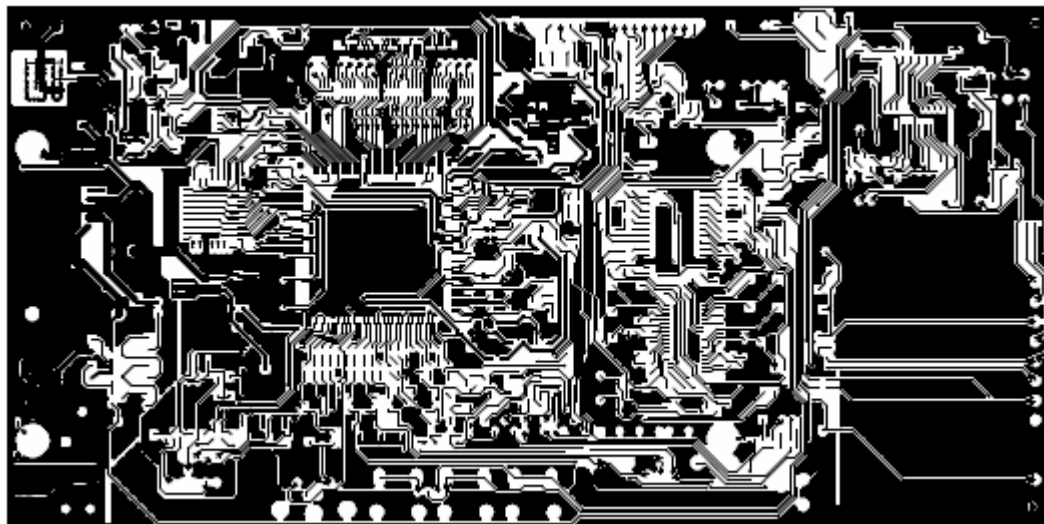
Part1:



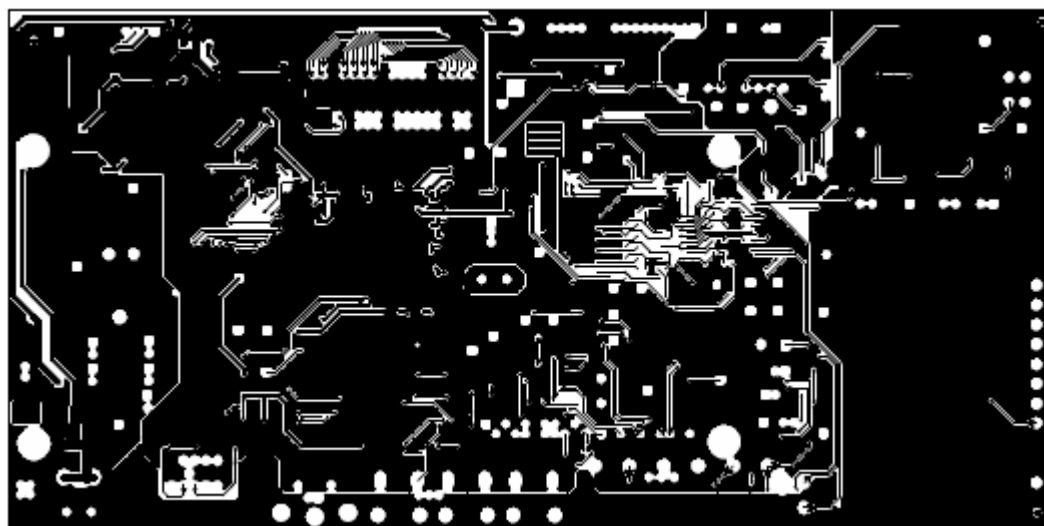
Schematic Diagram

Printed Circuit

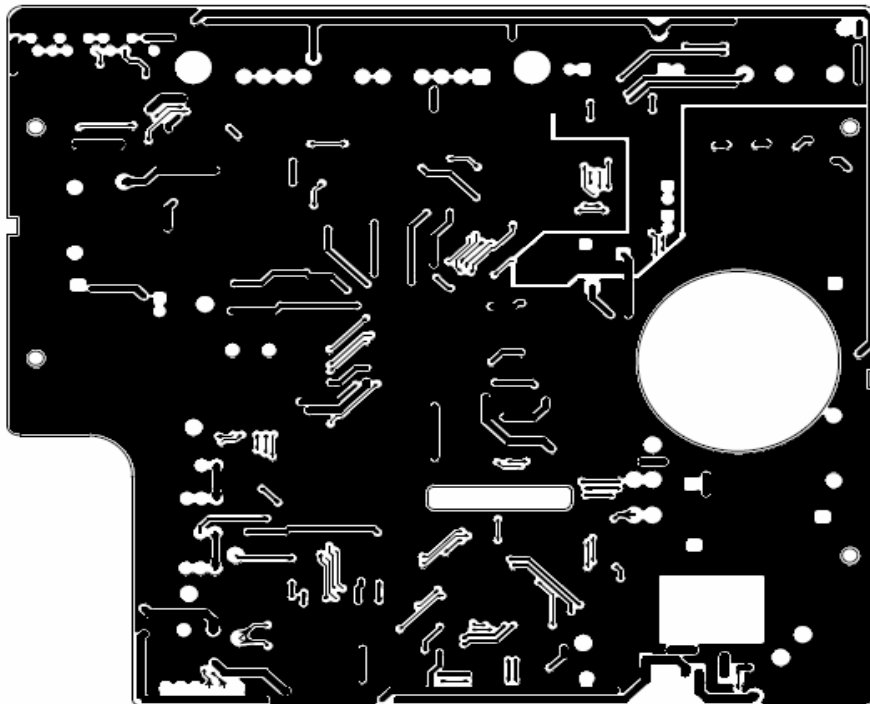
TV Main Board (Top View)



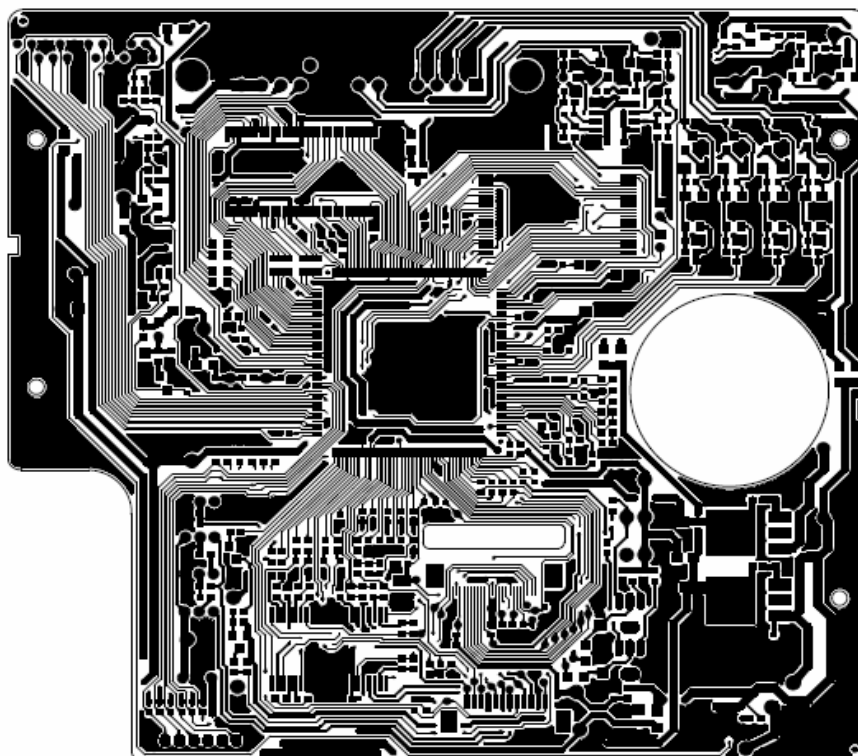
TV Main Board (Bottom view)



DVD Board (top view)

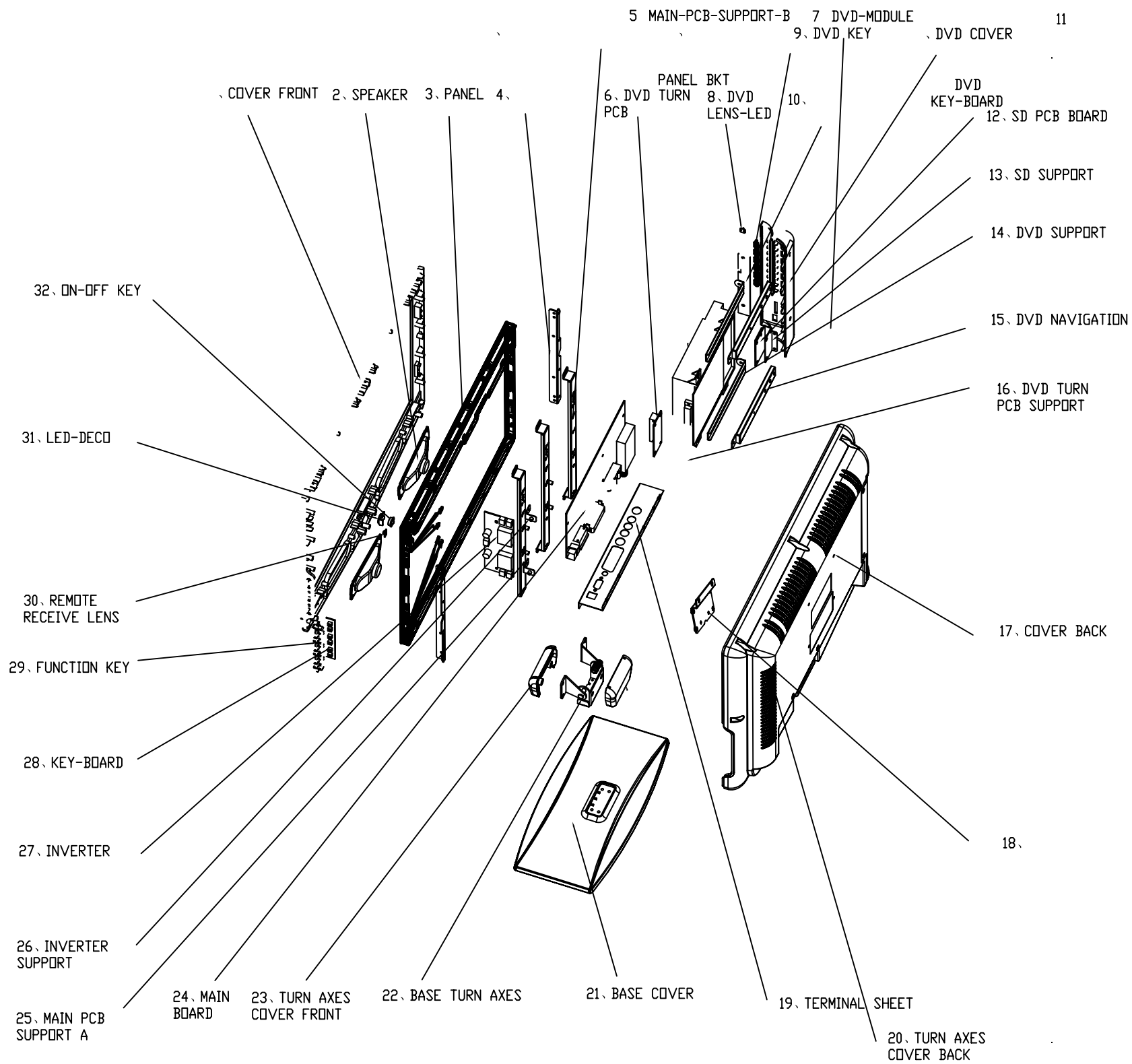


DVD Board(bottom view)



Part2:

Exploded view





150Khz, 3A PWM Buck Switching Regulator

Preliminary

■ General Description

The KP1500 series are monolithic integrated circuits that provide all the active functions for a step-down DC/DC converter, capable of driving a 3A load without additional transistor component. Requiring a minimum number of external component, the board space can be saved easily. The external shutdown function can be controlled by TTL logic level and then come into standby mode. The internal compensation makes feedback control have good line and load regulation without external design. Regarding protected function, thermal shutdown is to prevent over temperature operating from damage, and current limit is against over current operating of the output switch. The KP1500 series operates at a switching frequency of 150Khz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Other features include a guaranteed $\pm 4\%$ tolerance on output voltage under specified input voltage and output load conditions, and $\pm 15\%$ on the oscillator frequency. The output version included fixed 3.3V, 5V, 12V, and an adjustable type. The packages are available in a standard 5-lead TO-220(T) package and a 5-lead TO-263(U).

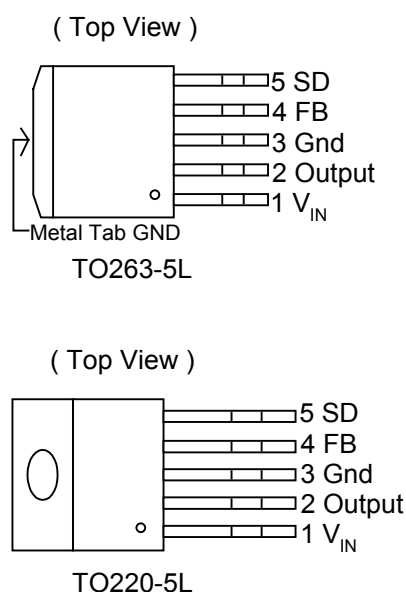
■ Features

- 3.3V, 5V, 12V and adjustable output versions
- Adjustable version output voltage range, 1.23V to 28V $\pm 4\%$ max over line and load condition
- Available in TO220-5L and TO263-5L packages
- Voltage mode non-synchronous PWM control
- Thermal-shutdown and current-limit protection
- ON/OFF shutdown control input
- Input voltage range up to 32V
- Output load current: 3A
- 150 kHz fixed frequency internal oscillator
- Low power standby mode
- Built-in switching transistor on chip

■ Applications

- Simple High-efficiency step-down(buck) regulator
- Efficient preregulator for linear regulators
- On-card switching regulators
- Positive to negative converter
- Battery Charger

■ Pin Assignments



■ Pin Descriptions

Name	Description
V_{IN}	Operating voltage input
Output	Switching output
Gnd	Ground
FB	Output voltage feedback control
SD	ON/OFF Shutdown

AP1084

5A Low Dropout Positive Adjustable or Fixed-Mode Regulator

■ Features

- 1.4V maximum dropout at full load current
- Built-in thermal shutdown
- Output current limiting
- Adjustable output voltage or fixed 1.5V, 1.8V, 2.5V, 3.3V, 5.0V
- Fast transient response
- Good noise rejection
- Package : TO252, TO263, TO220

■ General Description

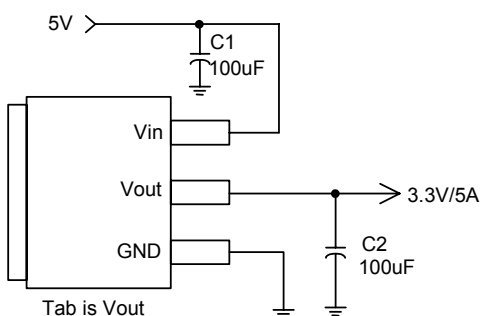
AP1084 is a low dropout positive adjustable or fixed-mode regulator with minimum of 5.0A output current capability. The product is specifically designed to provide well-regulated supply for low voltage IC applications such as high-speed bus termination and low current 3.3V logic supply. AP1084 is also well suited for other applications such as VGA cards. AP1084 is guaranteed to have lower than 1.4V dropout at full load current making it ideal to provide well-regulated outputs of 1.25 to 3.3V with 4.7 to 12V input supply.

■ Ordering Information

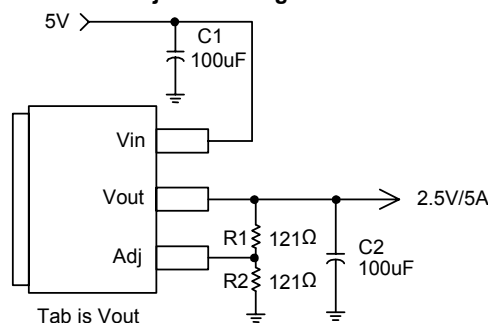
AP1084 X X X				
Low Dropout Regulator	Package	Vout	Lead Free	Packing
	D : TO252-3L K : TO263-3L T : TO220-3L	Blank : Adj 15 = 1.5V 18 = 1.8V 25 = 2.5V 33 = 3.3V 50 = 5.0V	Blank : Normal L : Lead Free Package	Blank : Tube A : Taping

■ Typical Circuit

5.0V to 3.3V Fixed Mode Regulator



Adjustable Regulator



Note: $V_o = V_{REF} * (1 + \frac{R_2}{R_1})$

AP1117

1A Low Dropout Positive Adjustable or Fixed-Mode Regulator

■ Features

- 1.4V maximum dropout at full load current
- Fast transient response
- Output current limiting
- Built-in thermal shutdown
- Packages: SOT223, TO263, TO252, TO220, SOT89
- Good noise rejection
- 3-Terminal Adjustable or Fixed 1.5V, 1.8V, 1.9V, 2.5V, 3.3V, 5.0V

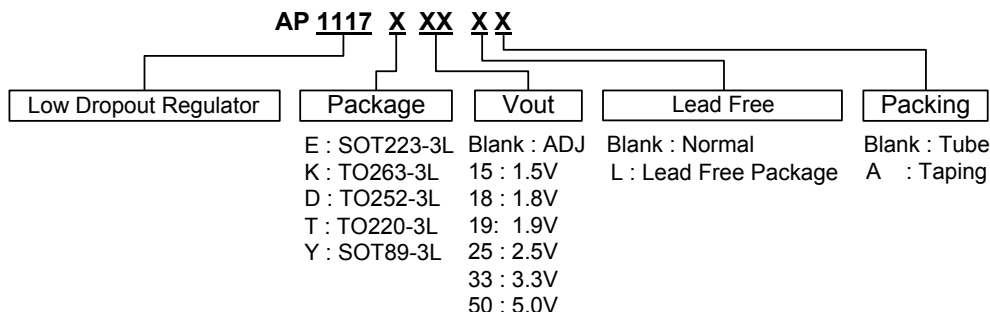
■ Applications

- PC peripheral
- Communication

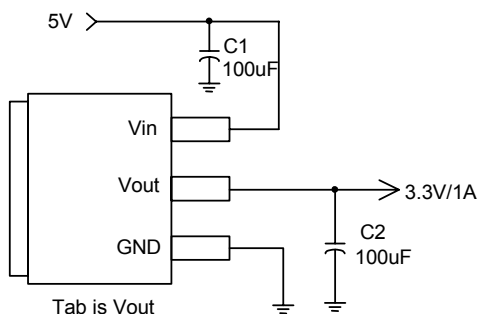
■ General Description

AP1117 is a low dropout positive adjustable or fixed-mode regulator with minimum of 1A output current capability. The product is specifically designed to provide well-regulated supply for low voltage IC applications such as high-speed bus termination and low current 3.3V logic supply. AP1117 is also well suited for other applications such as VGA cards. AP1117 is guaranteed to have lower than 1.4V dropout at full load current making it ideal to provide well-regulated outputs of 1.25 to 5.0 with 6.4V to 12V input supply.

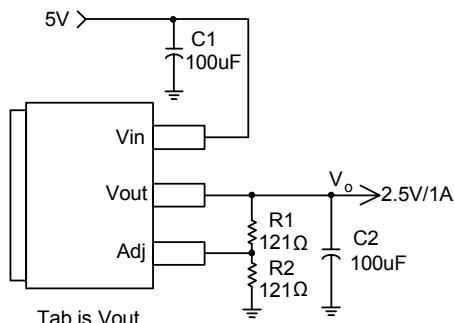
■ Ordering Information



■ Typical Circuit



(5V/3.3V fixed output)



(5V/2.5V ADJ output)

Note: $V_o = V_{REF} * (1 + \frac{R_2}{R_1})$

EN29LV040A**4 Megabit (512K x 8-bit) Uniform Sector,
CMOS 3.0 Volt-only Flash Memory****FEATURES**

- Fully compatible with EN29LV040
- Single power supply operation
 - Full voltage range: 2.7-3.6 volt read and write operations for battery-powered applications.
 - Regulated voltage range: 3.0-3.6 volt read and write operations for high performance 3.3 volt microprocessors.
- High performance
 - Access times as fast as 45 ns
- Low power consumption (typical values at 5 MHz)
 - 7 mA typical active read current
 - 15 mA typical program/erase current
 - 1 μ A typical standby current (standard access time to active mode)
- Flexible Sector Architecture:
 - Eight 64 Kbyte sectors
 - Supports full chip erase
 - Individual sector erase supported
 - Sector protection and unprotection: Hardware locking of sectors to prevent program or erase operations within individual sectors
- High performance program/erase speed
 - Byte/Word program time: 8 μ s typical
 - Sector erase time: 500ms typical
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Single Sector and Chip Erase
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes: Read or program another Sector during Erase Suspend Mode
- triple-metal double-poly triple-well CMOS Flash Technology
- Low Vcc write inhibit $\leq 2.5\text{V}$
- minimum 100K program/erase endurance cycle
- Package options
 - 8mm x 20mm 32-pin TSOP (Type 1)
 - 8mm x 14mm 32-pin TSOP (Type 1)
 - 32-pin PLCC
- Commercial and industrial Temperature Range

GENERAL DESCRIPTION

The EN29LV040A is a 4-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 524,288 bytes. Any byte can be programmed typically in 8 μ s. The EN29LV040A features 3.0V voltage read and write operation, with access times as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29LV040A has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.



CONNECTION DIAGRAMS

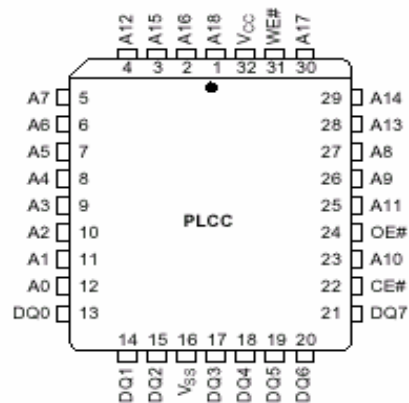
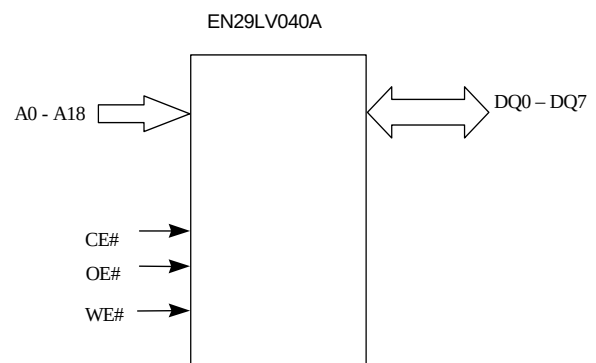


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A18	Addresses
DQ0-DQ7	8 Data Inputs/Outputs
WE#	Write Enable
CE#	Chip Enable
OE#	Output Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

FIGURE 1. LOGIC DIAGRAM



2 × 6 W stereo power amplifier**TDA1517; TDA1517P****FEATURES**

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs ($V_P = 0$ V)
- No switch-on/switch-off plop
- Electrostatic discharge protection.

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin (SIL9MPF) and a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for multi-media applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{sb}	standby current		–	0.1	100	μ A
I_{sw}	switch-on current		–	–	40	μ A
$ Z_i $	input impedance		50	–	–	k Ω
P_o	output power	$R_L = 4 \Omega$; THD = 0.5%	–	5	–	W
		$R_L = 4 \Omega$; THD = 10%	–	6	–	W
SVRR	supply voltage ripple rejection	$f_i = 100$ Hz to 10 kHz	48	–	–	dB
α_{cs}	channel separation		40	–	–	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		–	50	–	μ V
T_c	crystal temperature		–	–	150	$^{\circ}$ C

ORDERING INFORMATION

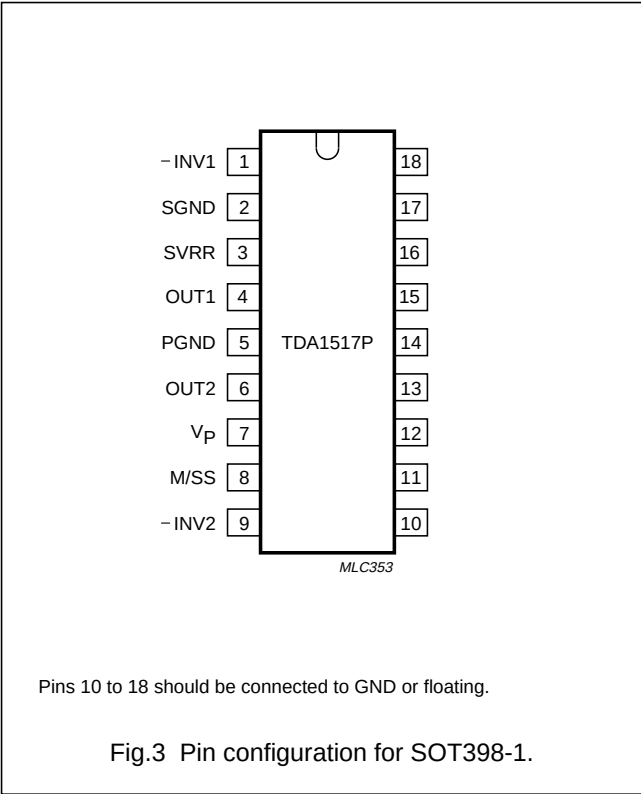
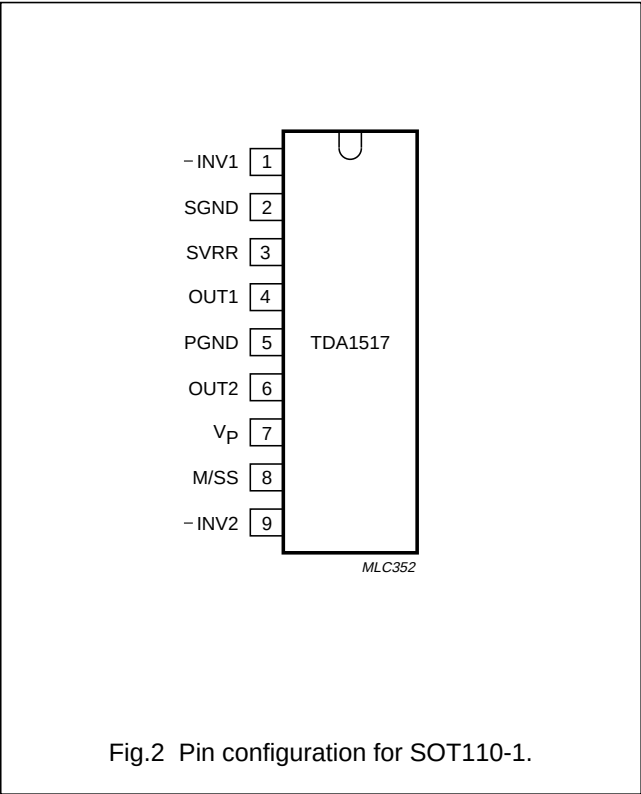
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA1517P	HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1

2 × 6 W stereo power amplifier

TDA1517; TDA1517P

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V _P	7	supply voltage
M/SS	8	mute/standby switch input
–INV2	9	non-inverting input 2

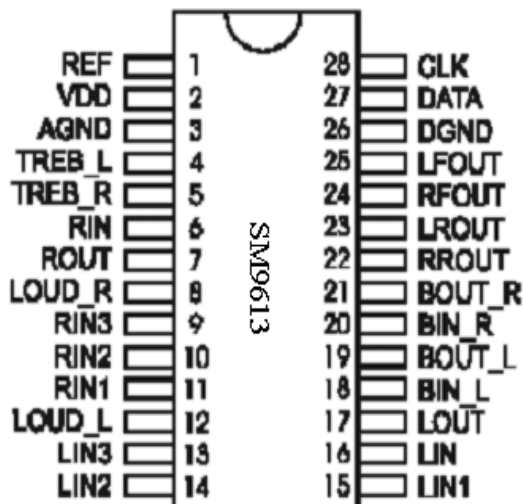
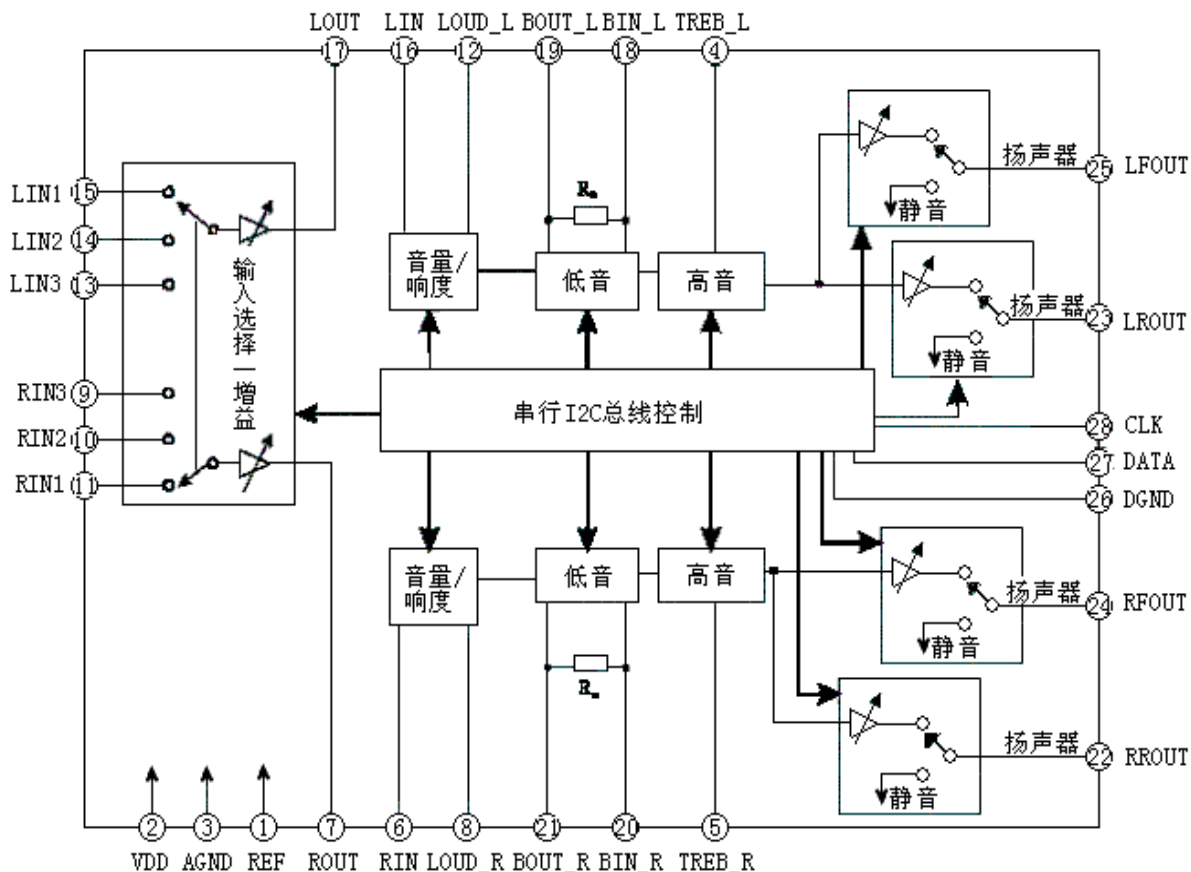


FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of the device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

SM9613



2-wire Serial EEPROM 32K/64K AF24BC32/64

FEATURES:

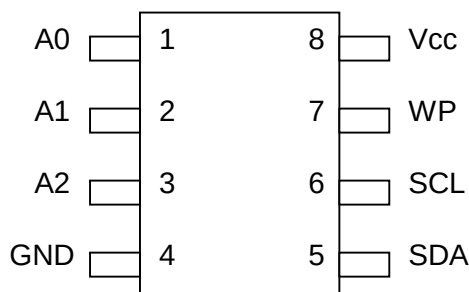
- Internally organized as 4096 x 8 (32K), 8192 x 8 (64K)
- Low-voltage and standard-voltage operation : 1.8 to 5.5 V
- 2-wire serial interface bus
- Data retention: 100 years
- High endurance: 1,000,000 Write Cycles
- 100 kHz (1.8V) & 400kHz (2.7V, 5V) compatibility
- Self-timed write cycle (5ms max)
- Bi-directional data transfer protocol
- Write protect pin for hardware data protection
- 32-byte page write modes
- Allows for partial page writes
- 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP, 8-lead MSOP (AF24BC32) Packages

DESCRIPTION

Aplus Flash Technology's AF24BC32/64 provides 32K/64K of serial electrically erasable and programmable read-only memory (EEPROM). The wide V_{dd} range allows for low-voltage operation down to 1.8V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The AF24BC32/64 is available in 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP and 8-lead MSOP (AF24BC32) packages and is accessed via a 2-wire serial interface.

Figure 1. Pin Configurations

8-pin PDIP/TSSOP/SOIC/MSOP



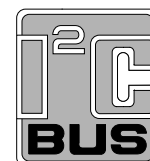
Pin Name	Function
A0 – A2	Address inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
Vcc	Power Supply

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

1 FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C-bus
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled



- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module Address (MAD)
- Four I²C-bus addresses via MAD.

2 GENERAL DESCRIPTION

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

3 APPLICATIONS

- TV, VTR, PC and STB applications.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V3	HVQFN32	plastic, heatsink very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1
TDA9886T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

TDA9885; TDA9886

7 PINNING

SYMBOL	PIN			DESCRIPTION
	TDA9886T TDA9886TS	TDA9885T TDA9885TS	TDA9885HN	
VIF1	1	1	30	VIF differential input 1
VIF2	2	2	31	VIF differential input 2
n.c.	–	–	32	not connected
OP1	3	3	1	output port 1; open-collector
FMPLL	4	4	2	FM-PLL for loop filter
DEEM	5	5	3	de-emphasis output for capacitor
AFD	6	6	4	AF decoupling input for capacitor
DGND	7	7	5	digital ground
n.c.	–	–	6	not connected
AUD	8	8	7	audio output
TOP	9	9	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	I ² C-bus data input and output
SCL	11	11	10	I ² C-bus clock input
SIOMAD	12	12	11	sound intercarrier output and MAD select with resistor
n.c.	–	–	12	not connected
n.c.	13	13	13	not connected
n.c.	–	–	14	not connected
TAGC	14	14	15	tuner AGC output
REF	15	15	16	4 MHz crystal or reference signal input
VAGC	16	–	–	VIF-AGC for capacitor
n.c.	–	16	17	not connected
CVBS	17	17	18	composite video output
n.c.	–	–	19	not connected
AGND	18	18	20	analog ground
VPLL	19	19	21	VIF-PLL for loop filter
V _P	20	20	22	supply voltage
AFC	21	21	23	AFC output
OP2	22	22	24	output port 2; open-collector
n.c.	–	–	25	not connected
SIF1	23	23	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	not connected
n.c.	–	–	29	not connected

SHANGHAI JINXIN ELECTRONICS LTD.	MODEL UVL7605VMW	
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1. SCOPE.

This specification applies to VHF and UHF tuner model
UVL7605VMW

2. INPUT IMPEDANCE AND OUTPUT IMPEDANCE

Input impedance: 75 Ohm unbalanced

Output impedance: 75 Ohm unbalanced

3. INTERMEDIATE FREQUENCY

Picture carrier: 45.75MHz

Sound carrier: 41.25MHz

4. Receiving Channel

Ch.2~B

Ch.C~W+11

Ch.W+12~69

5. STANDARD SUPPLY VOLTAGE AND CURRENT.

[illegible]

6. Maximum supply voltage

No.	Terminal name	Maximum supply voltage (V)
1	AGC	+4.5V, DC
3	AS	+5.5V, DC
4	SCL	+5.5V, DC
5	SDA	+5.5V, DC
6	+B	+5.5V, DC
7	BP	+5.5V, DC
9	BT	+34V, DC

7. Operation guaranteed voltage

No.	Terminal name	Supply voltage
1	AGC	0~4.0V, DC
3	AS	0~5.25V, DC
4	SCL	0~5.25V, DC
5	SDA	0~5.25V, DC
6	+B	+5.0V±0.25V, DC
7	BP	+5.0V±0.25V, DC
9	BT	+32V±1V, DC

8. Temperature range

Operation guaranteed temperature: $-10^{\circ}\text{C} \sim +60^{\circ}\text{C}$

Storage temperature: $-10^{\circ}\text{C} \sim +70^{\circ}\text{C}$

9. Construction and mechanical characteristics.

External connection terminals

SHANGHAI JINXIN
ELECTRONICS LTD.

SPECIFICATION
UVL7605VMW

No.	Terminal name	Terminal Description
1	AGC	VHF/UHF AGC Terminal
2	VT	Tuning Voltage monitor
3	AS	Address Select
4	SCL	Serial Clock Line
5	SDA	Serial Data Line
6	+B	5V supply voltage
7	BP	Internal connection to pin 6
9	BT	Tuning Voltage Supply
10	IF1	IF Output (balanced)
11	IF2	IF Output (balanced)
12	U /V ANT	VHF/UHFANT Terminal

10. STANDRAD TEST CONDITIONS

Unless otherwise specified, the tests shall be carried out at the temperature of $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$ and relative humidity of $65\% \pm 15\%$

11.ELECTRICAL CHARATERISTICS

11.1 Power gain

	Min	Typ	Max	Unit
VHF L	32	35		dB
VHF H	32	35		dB
UHF	32	35		dB

11.2 Gain variation

	Min	Typ	Max	Unit
VHF L			8.0	dB
VHF H			8.0	dB
UHF			8.0	dB

11.3 Noise figure

	Min	Typ	Max	Unit
VHF L		5.0	9.0	dB
VHF H		5.0	9.0	dB
HF		5.0	9.0	dB

UTC 78DXX LINEAR INTEGRATED CIRCUIT

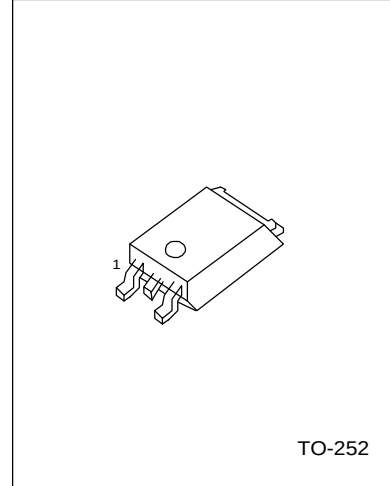
3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATOR

DESCRIPTION

The UTC 78DXX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 0.5 A.

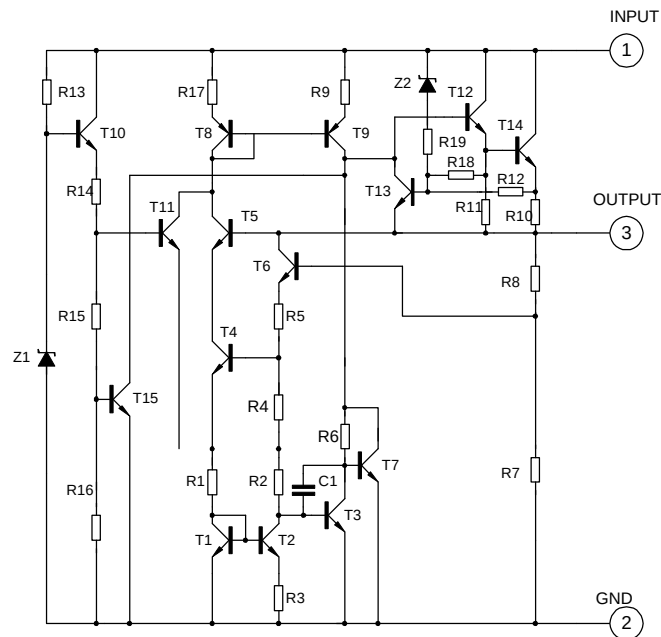
FEATURE

- *Output current up to 0.5 A
- *Fixed output voltage of 5V, 6V, 8V, 9V, 12V, 15V, 18V and 24V available
- *Thermal overload shutdown protection
- *Short circuit current limiting
- *Output transistor SOA protection



1:Input 2:GND 3:Output

EQUIVALENT CIRCUIT



UTC UNISONIC TECHNOLOGIES CO. LTD

Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

FEATURES

- Wide analog input voltage range from -5 V to $+5\text{ V}$
- Low ON-resistance:
 - $80\ \Omega$ (typical) at $V_{CC} - V_{EE} = 4.5\text{ V}$
 - $70\ \Omega$ (typical) at $V_{CC} - V_{EE} = 6.0\text{ V}$
 - $60\ \Omega$ (typical) at $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation: to enable 5 V logic to communicate with $\pm 5\text{ V}$ analog signals
- Typical “break before make” built in
- Complies with JEDEC standard no. 7A
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V .
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating.

DESCRIPTION

The 74HC4052 and 74HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4052B. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4052 and 74HCT4052 are dual 4-channel analog multiplexers or demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin $\bar{E}$). When pin $\bar{E} = \text{LOW}$, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin $\bar{E} = \text{HIGH}$, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

V_{CC} and GND are the supply voltage pins for the digital control inputs (pins S0, S1, and $\bar{E}$). The V_{CC} to GND ranges are 2.0 V to 10.0 V for 74HC4052 and 4.5 V to 5.5 V for 74HCT4052. The analog inputs/outputs (pins nY0 to nY3 and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V .

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

FUNCTION TABLE

INPUT ⁽¹⁾			CHANNEL BETWEEN
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

Note

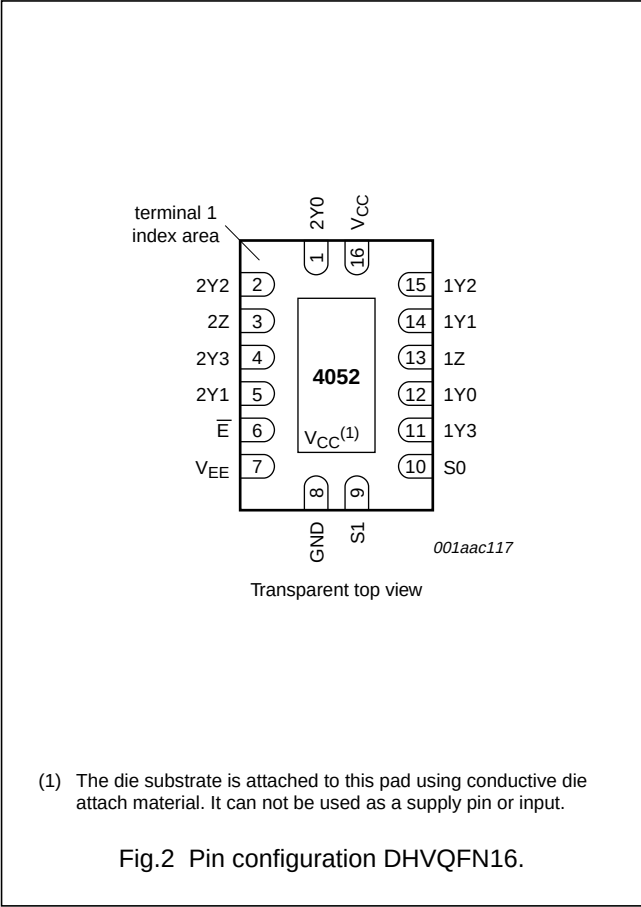
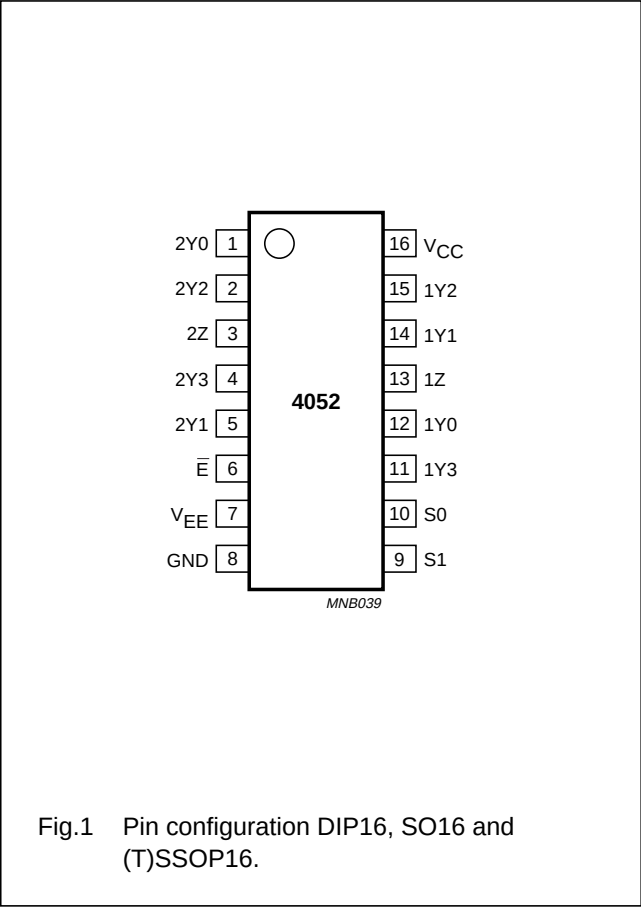
1. H = HIGH voltage level
L = LOW voltage level
X = don't care.

Dual 4-channel analog multiplexer,
demultiplexer

74HC4052; 74HCT4052

PINNING

PIN	SYMBOL	DESCRIPTION
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	$\overline{E}$	enable input (active LOW)
7	V _{EE}	negative supply voltage
8	GND	ground (0 V)
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V _{CC}	positive supply voltage





PRELIMINARY PRODUCT BRIEF

FLI8125

Single-Chip LCD TV Controller

APPLICATION

- Cost Effective, Large Screen LCD TVs
- Portable / Handheld LCD TVs
- Small Screen Video Displays

FEATURES

- Faroudja DCDi – Edge™
- Integrated Triple ADC
- Digital Input Port
- Scaling Engine
- Image Enhancement
- Digital Output
- OSD Controller
- Embedded Microprocessor
- VBI Slicer
- JTAG Support

PACKAGE

- 208 PQFP

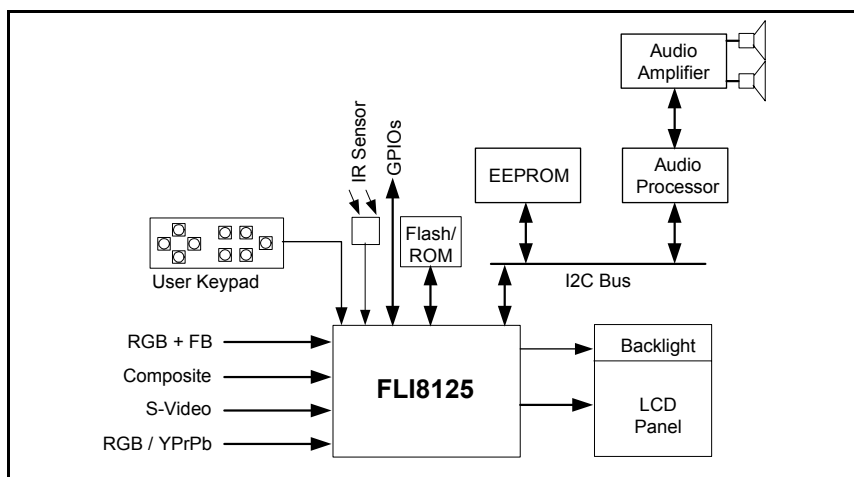
DESCRIPTION

The FLI8125 is a highly integrated cost effective mixed signal solution for LCD TV and Digital Video applications. Capable of meeting global broadcast market requirements, the FLI8125 incorporates a multi-standard video decoder, high-speed triple 8-bit Analog-to-Digital Converter (ADC), and front end switching. The integrated VBI Slicer adds Closed Captioning (CC) and Teletext service support, and the integrated microprocessor enables full system control without external devices.

The FLI8125 can capture and process both video and RGB graphics streams. The multi-standard video decoder is capable of accepting NTSC, PAL or SECAM and other sub-formats. The integrated ADC accepts both analog RGB and YPrPb inputs.

Interlaced video signals are converted into progressive scan signals using a memory-less deinterlacing technique. Progressive scan signals are then passed to the Faroudja DCDi – Edge suite for further image processing. Faroudja DCDi – Edge incorporates Faroudja's patented and Emmy award winning Edge Correction technology eliminating objectionable staircasing on diagonal lines; Horizontal Enhancement technology is used to make an image look crisper and more realistic; Adaptive Contrast and Color (ACC) enables dynamic contrast enhancement and color saturation correction; and Active Color Management-II (ACM-II) enables color correction for subtle changes in color that can dramatically improve the image (e.g., flesh tone, green stretch, etc.). A fully programmable 3x3 matrix provides color space conversion and global color correction technology. Programmable Color Look Up Tables (CLUT) provides gamma correction of the output signal. Combined, these features facilitate accurate color reproduction that enables use of the full dynamic range on any fixed pixel display device.

FLI8125 BASED "SMART" VIDEO DISPLAY

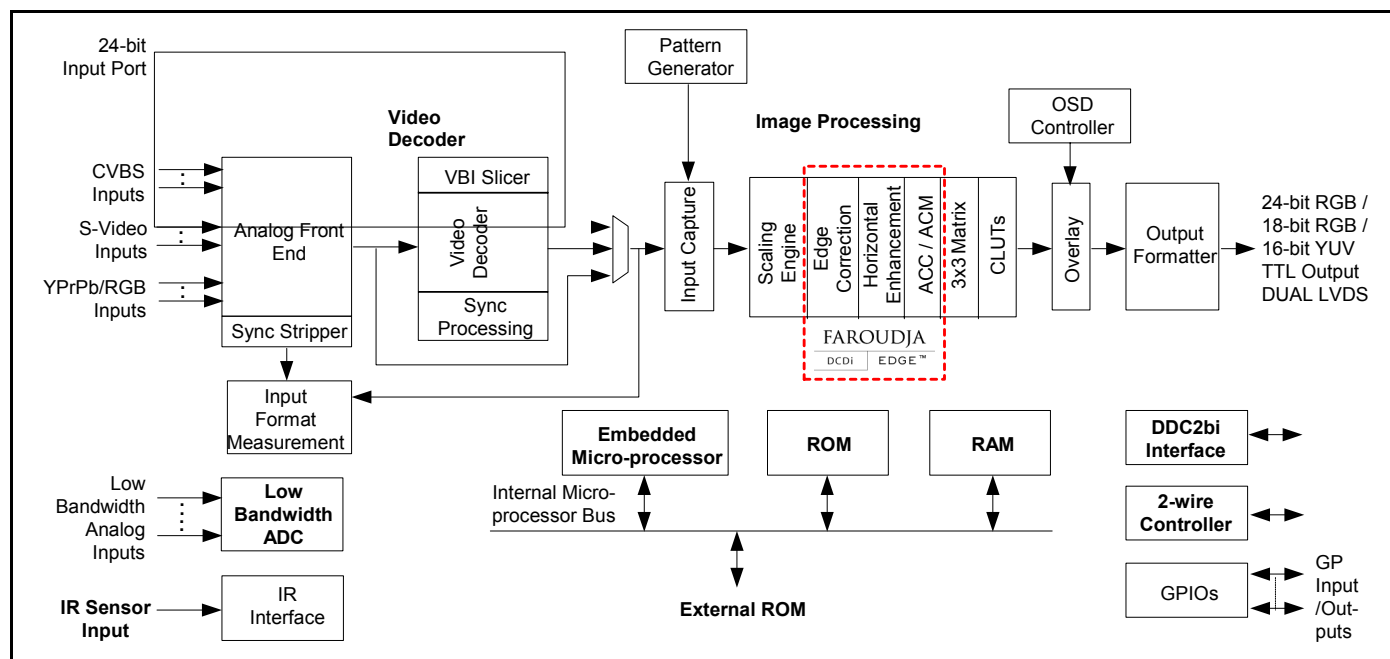


FAROUDJA

DCDi

EDGE™

FLI8125 FUNCTIONAL BLOCK DIAGRAM



FLI8125 FEATURE DESCRIPTIONS

INTEGRATED TRIPLE ADC

- RGB / YPbPr support up to 135MHz
- SCART – RGB + Fast Blank support
- Interlaced and progressive scan
- External OSD support

DIGITAL INPUT PORT

- 24-bit re-configurable input port

INTEGRATED 2D VIDEO DECODER

- Worldwide NTSC/PAL/SECAM support
- Macrovision / VCR trick mode support

EMBEDDED MICROPROCESSOR

- Turbo 186 core
- Internal RAM / ROM
- Serial Flash / Parallel ROM support
- 2-wire slave controller, UART support
- Internal RESET Controller
- GPIOs , Low Bandwidth ADC – 6 input
- Infra-red Interface

SCALING ENGINE

- Independent H & V scaling factors
- 4:2:2 YPbPr or 4:4:4 RGB scaling
- Anamorphic scaling (non-linear)

FAROUDJA DCDI – EDGE™

- Edge Correction
 - Eliminates objectionable stair-casing
 - Enhances clarity and realism
- Horizontal Enhancement
- Adaptive Contrast and Color (ACC)
- Active Color Management - II (ACM-II)

DIGITAL OUTPUT

- 18/24-bit 85Mhz TTL output
- Dual LVDS up to SXGA
- Energy Spectrum Management for reducing EMI
- Programmable CLUT for gamma correction

OSD CONTROLLER

- Up to 4 windows: 1, 2 or 4-bits per pixel color
- Programmable Font scalar to meet Teletext requirements

VBI SLICER

- V-Chip, Closed Captioning, XDS, CGMS, WSS decode
- Teletext 1.5 support

JTAG SUPPORT

- Boundary Scan support

2 Pin Diagram

The FLI8125 device is packaged in a 208-pin Plastic Quad Flat Pack (PQFP).

Figure 2: FLI8125 Pinout



3 Pin List

I/O Legend: **A** = Analog, **I** = Input, **O** = Output, **P** = Power, **G**= Ground

Table 1: Analog Input Port

Pin Name	No.	I/O	Description
VDD18_AB	158	AP	Analog Power (1.8V) for A & B Channels. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
NC	159		No Connection. Leave this pin open for normal operation.
GND18_C	160	AG	Analog Ground (1.8V Return) for C channel. Must be directly connected to the analog system ground plane on board.
VDD18_C	161	AP	Analog Power (1.8V) for C Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
ADC_TEST	162	O	Analog Front End Test O/P. Leave this Pin open. Used for factory testing purpose only.
AVDD_ADC	163	AP	Analog Power (3.3V) for ADC. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AGND	164	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
AGND	165	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV1P	166	AI	Positive analog sync input for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	167	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A1P	168	AI	Positive analog input 'A' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	169	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B1P	170	AI	Positive analog input 'B' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	171	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C1P	172	AI	Positive analog input 'C' for channel 1. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_A	173	AP	Analog Power (3.3V) for ADC of Channel-A. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
AN	174	AI	Negative analog input 'A' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-A Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	175	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV2P	176	AI	Positive analog sync input for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	177	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A2P	178	AI	Positive analog input 'A' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	179	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B2P	180	AI	Positive analog input 'B' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	181	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C2P	182	AI	Positive analog input 'C' for channel 2. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_B	183	AP	Analog Power (3.3V) for ADC of Channel-B. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
BN	184	AI	Negative analog input 'B' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-B Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	185	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV3P	186	AI	Positive analog sync input for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.

Pin Name	No.	I/O	Description
GNDS	187	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A3P	188	AI	Positive analog input 'A' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	189	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B3P	190	AI	Positive analog input 'B' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	191	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C3P	192	AI	Positive analog input 'C' for channel 3. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_C	193	AP	Analog Power (3.3V) for ADC of Channel-C. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
CN	194	AI	Negative analog input 'C' for channels 1 through 4. This acts as the return Path for the Sources connected to Channel-C Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
AGND	195	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
SV4P	196	AI	Positive analog sync input for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	197	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
A4P	198	AI	Positive analog input 'A' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	199	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
B4P	200	AI	Positive analog input 'B' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
GNDS	201	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
C4P	202	AI	Positive analog input 'C' for channel 4. The input has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network.
AVDD_SC	203	AP	Analog Power (3.3V) for ADC of SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
SVN	204	AI	Negative analog sync input for channels 1 through 4. This acts as the return Path for the Sources connected to SV Channel Inputs. This has to be AC coupled using a series 20 Ohm resistor and 0.1uF Capacitor network to Analog Ground Plane on board.
VO_GND	205	AG	Analog Ground. Must be directly connected to the analog system ground plane on board.
VOUT2	206	AO	Analog VOUT signal This is the Analog Video Output from the Decoder in the Composite Video format. This can be amplified and be fed to any video display device.
VDD18_SC	207	AP	Analog Power (1.8V) for SYNC Channel. Must be bypassed with 0.1uF capacitor to the analog system ground plane.
GND18_SC	208	AG	Analog Ground (1.8V Return) for SYNC channel. Must be directly connected to the analog system ground plane on board.

Table 2: Low Bandwidth ADC Input Port

Pin Name	No	I/O	Description
VDDA33_LBADC	1	AP	Analog Power (3.3V) for Low Bandwidth ADC Block. Must be bypassed with 0.1uF capacitor.
LBADC_IN1	2	AI	Low Bandwidth Analog Input-1. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN2	3	AI	Low Bandwidth Analog Input-2. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN3	4	AI	Low Bandwidth Analog Input-3. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN4	5	AI	Low Bandwidth Analog Input-4. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN5	6	AI	Low Bandwidth Analog Input-5. The Input signal connected to this Pin, must be bypassed with a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_IN6	7	AI	Low Bandwidth Analog Input-6. The Input signal connected to this Pin, must be bypassed with

Pin Name	No	I/O	Description
			a 0.1uF capacitor and could be in the range of 0V to 3.3V (peak to peak).
LBADC_RTN	8	AG	This Pin provides the Return Path for LBADC inputs. Must be directly connected to the analog system ground plane on board.
VSSA33_LBADC	9	AG	Analog Ground for Low Bandwidth ADC Block. Must be directly connected to the analog system ground plane on board.

Table 3: RCLK PLL Pins

Pin Name	No	I/O	Description
GND_RPLL	11	DG	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD_RPLL_18	12	DP	Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to Ground Plane.
VBUFC_RPLL	13	O	Test Output. Leave this Pin Open. This is reserved for Factory Testing Purpose.
AGND_RPLL	14	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
XTAL	15	AO	Crystal oscillator output.
TCLK	16	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator.
AVDD_RPLL_33	17	AP	Analog Power (3.3V) for RCLK PLL. Must be bypassed with 0.1uF capacitor.

Table 4: Digital Video Input Port

Pin Name	No	I/O	Description
VID_CLK_1	153	I	Video port data clock input meant for Video Input – 1. Up to 75Mhz [Input, 5V-tolerant]
VIDIN_HS	122	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Horizontal Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Horizontal Sync Input for Video Input – 1. OR this Pin acts as Horizontal Sync Input for 24 Bit Video Input
VIDIN_VS	121	I	When Video Input – 1 is in BT656 Mode, this Pin acts as Vertical Sync Input for Video Input – 2. OR when Video Input – 1 is in 16 Bit Mode this Pin acts as Vertical Sync Input for Video Input – 1. OR this Pin acts as Vertical Sync Input for 24 Bit Video Input
VID_DATA_IN_0 VID_DATA_IN_1 VID_DATA_IN_2 VID_DATA_IN_3 VID_DATA_IN_4 VID_DATA_IN_5 VID_DATA_IN_6 VID_DATA_IN_7	135 136 137 138 139 140 141 142	IO	Input YUV data in 8-bit BT656 of Video Input – 1 [Bi-Directional, 5V-tolerant] OR Input Y Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Red Data in case of 24 Bit Video Input
VID_DATA_IN_8 VID_DATA_IN_9 VID_DATA_IN_10 VID_DATA_IN_11 VID_DATA_IN_12 VID_DATA_IN_13 VID_DATA_IN_14 VID_DATA_IN_15	145 146 147 148 149 150 151 152	IO	Input Pr / Pb Data in case of 16 Bit Video Input (CCIR601) of Video Input – 1 OR Input Green Data in case of 24 Bit Video Input
VID_DATA_IN_16 VID_DATA_IN_17 VID_DATA_IN_18 VID_DATA_IN_19 VID_DATA_IN_20 VID_DATA_IN_21 VID_DATA_IN_22 VID_DATA_IN_23	123 124 125 128 129 130 131 132	IO	Input Blue Data in case of 24 Bit Video Input OR Video Input – 2 in 8-bit with Embedded Sync / Separate Sync in which case VID_DATA_IN_16 acts as the LSB of the 8-bit Video input and VID_DATA_IN_23 acts as the MSB of the 8-bit Video input.

Pin Name	No	I/O	Description
VID_CLK2	118	I	Video port data clock input meant for Video Input – 2. Up to 75Mhz [Input, 5V-tolerant]
VID_DE/FLD	115	I	Video Active Signal Input or the Field Signal Input from external Digital Video Source.

Note: In case of Multiple Digital Video Input Sources, only one source could be in 8-Bit with embedded Sync (BT656 mode) format.

Table 5: System Interface

Pin Name	No	I/O	Description
RESETn	10	I	Hardware Reset (active low) [Schmitt trigger, 5v-tolerant] Connect to ground with 0.01uF (or larger) capacitor.
TEST	20	I	For normal mode of operation connect this Pin to Ground.
GPIO15	21	IO	This pin is available as a general-purpose input/output port. Also it is optionally programmable to give out the external chip select signal meant for external SRAM. Refer to note below.
HSYNC2	22	I	Horizontal Sync signal Input-2. Used when Analog RGB component signal carries separate HSYNC signal.
VSYNC2	23	I	Vertical Sync signal Input-2. Used when Analog RGB component signal carries separate VSYNC signal.
HOST_SCLK	24	IO	Host input clock or 186 UART Data In or JTAG clock signal. [Input, Schmitt trigger, 5V-tolerant]
HOST_SDATA	25	IO	Host input data or 186 UART Data Out or JTAG mode signal. [Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant]
DDC_SCLK	26	IO	DDC2Bi clock for VGA Port [internal 10KΩ pull-up resistor]
DDC_SDATA	27	IO	DDC2Bi data for VGA Port [internal 10KΩ pull-up resistor]
MSTR_SCLK	30	O	Clock signal from Master Serial 2 Wire Interface Controller
MSTR_SDATA	31	IO	Data signal meant for Master Serial 2 Wire interface Controller
TCK	34	IO	This Pin accepts the Input Clock signal in case of Boundary Scan Mode.
TDI	35	IO	This Pin accepts the Input Data signal in case of Boundary Scan Mode.
TMS	36	IO	This Pin accepts the Input Test Mode Select signal in case of Boundary Scan Mode.
TRST	37	IO	This Pin accepts the Boundary Scan Reset signal in case of Boundary Scan Mode.
GPIO6/IRin	38	IO	Input from Infra Red Decoder can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO7/IRQin	41	IO	Input Interrupt Request signal can be connected to this Pin. When not used, this pin is available as General Purpose Input/output Port.
GPIO8/IRQout	42	IO	This Pin will give out the Interrupt Signal to interrupt external Micro. When not used, this pin is available as General Purpose Input/output Port.
GPIO9/SIPC_SCLK	43	IO	This Pin accepts the Clock signal from External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. When not used, this pin is available as General Purpose Input/output Port.
GPIO10/SIPC_SDATA/ A18	44	IO	This Pin acts as the Data I/O signal when used with External Serial 2 Wire interface Bus if FLI8125 is programmed to be in Slave mode. Or this Pin is programmable to give out Address # 18 from the Internal Micro when used with 512K External Memory. When not used, this pin is available as General Purpose Input/output Port.
GPIO11/PWM0	47	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO12/PWM1	48	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO13/PWM2	51	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. When not used, this pin is available as General Purpose Input/output Port.
GPIO14/PWM3/ SCART16	52	IO	This Pin can be programmed to give out Pulse Width Modulated Output Pulses for external use. Or it can be programmed to sense the Fast Blank Input signal from a SCART I/P source. When not used, this pin is available as General Purpose Input/output Port.
TDO	55	O	This Pin provides the Output Data in case of Boundary Scan Mode.
HSYNC1	156	I	Horizontal Sync signal Input-1. Used when Analog RGB component signal carries

Pin Name	No	I/O	Description
			separate HSYNC signal.
VSYNC1	157	I	Vertical Sync signal Input-1. Used when Analog RGB component signal carries separate VSYNC signal.
	101	O	Clock Output meant for External OSD Controller
	102	O	Horizontal Sync Output meant for External OSD Controller
XOSD_CLK	103	O	Vertical Sync Output meant for External OSD Controller
XOSD_HS	104	O	Field Signal Output meant for External OSD Controller
PD20/B4/GPIO0 PD21/B5/GPIO1 PD22/B6/GPIO2 PD23/B7/GPIO3	86 87 88 89	IO	These Pins provide the Panel Data as shown in the TTL Display Interface Table below. These are available as General Purpose Input / Output Pins when not used as Panel Data.

Table 6: LVDS Display Interface

Pin Name	No	I/O	Description
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]
AVDD_LV_33	56	DP	Digital Power for LVDS Block. Connect to digital 3.3V supply.
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.
AVSS_LV	58	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	59	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_E	60	O	These form the Differential Data Output for Channel – 3 (Even).
CH3N_LV_E	61	O	
CLKP_LV_E	62	O	These form the Differential Clock Output Even Channel.
CLKN_LV_E	63	O	
CH2P_LV_E	64	O	These form the Differential Data Output for Channel – 2 (Even).
CH2N_LV_E	65	O	
CH1P_LV_E	66	O	These form the Differential Data Output for Channel – 1 (Even).
CH1N_LV_E	67	O	
CH0P_LV_E	68	O	These form the Differential Data Output for Channel – 0 (Even).
CH0N_LV_E	69	O	
AVSS_OUT_LV	70	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	71	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.
CH3P_LV_O	72	O	These form the Differential Data Output for Channel – 3 (Odd).
CH3N_LV_O	73	O	
CLKP_LV_O	74	O	These form the Differential Clock Output Odd Channel.
CLKN_LV_O	75	O	
CH2P_LV_O	76	O	These form the Differential Data Output for Channel – 2 (Odd).
CH2N_LV_O	77	O	
CH1P_LV_O	78	O	These form the Differential Data Output for Channel – 1 (Odd).
CH1N_LV_O	79	O	
CH0P_LV_O	80	O	These form the Differential Data Output for Channel – 0 (Odd).
CH0N_LV_O	81	O	
AVSS_OUT_LV	82	G	Ground for LVDS outputs.
AVDD_OUT_LV_33	83	DP	Digital Power for LVDS outputs. Connect to digital 3.3V supply.

Table 7: TTL Display Interface

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PBIAS	53	O	Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant]	
PPWR	54	O	Panel Power Control [Tri-state output, 5V- tolerant]	
AVDD_LV_33	56	DP	Digital Power for TTL Block. Connect to digital 3.3V supply.	
VCO_LV	57	O	Reserved. Output for Testing Purpose only at Factory.	
AVSS_LV	58	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	59	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
R0	60	O	Red channel bit 0 (Even)	Not used.
R1	61	O	Red channel bit 1 (Even)	Not used.
R2	62	O	Red channel bit 2 (Even)	Red channel bit 0 (Even)
R3	63	O	Red channel bit 3 (Even)	Red channel bit 1 (Even)
R4	64	O	Red channel bit 4 (Even)	Red channel bit 2 (Even)
R5	65	O	Red channel bit 5 (Even)	Red channel bit 3 (Even)
R6	66	O	Red channel bit 6 (Even)	Red channel bit 4 (Even)
R7	67	O	Red channel bit 7 (Even)	Red channel bit 5 (Even)
G0	68	O	Green channel bit 0 (Even)	Not used.
G1	69	O	Green channel bit 1 (Even)	Not used.
AVSS_OUT_LV	70	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	71	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
G2	72	O	Green channel bit 2 (Even)	Green channel bit 0 (Even)
G3	73	O	Green channel bit 3 (Even)	Green channel bit 1 (Even)
G4	74	O	Green channel bit 4 (Even)	Green channel bit 2 (Even)
G5	75	O	Green channel bit 5 (Even)	Green channel bit 3 (Even)
G6	76	O	Green channel bit 6 (Even)	Green channel bit 4 (Even)
G7	77	O	Green channel bit 7 (Even)	Green channel bit 5 (Even)
B0	78	O	Blue channel bit 0 (Even)	Not used.
B1	79	O	Blue channel bit 1 (Even)	Not used.
B2	80	O	Blue channel bit 2 (Even)	Blue channel bit 0 (Even)
B3	81	O	Blue channel bit 3 (Even)	Blue channel bit 1 (Even)
AVSS_OUT_LV	82	G	Ground for TTL outputs.	
AVDD_OUT_LV_33	83	DP	Digital Power for TTL outputs. Connect to digital 3.3V supply.	
PD20/B4	86	O	Blue channel bit 4 (Even)	Blue channel bit 2 (Even)
PD21/B5	87	O	Blue channel bit 5 (Even)	Blue channel bit 3 (Even)
PD22/B6	88	O	Blue channel bit 6 (Even)	Blue channel bit 4 (Even)
PD23/B7	89	O	Blue channel bit 7 (Even)	Blue channel bit 5 (Even)
DEN	90	O	Display Data Enable	
DHS	91	O	Display Horizontal Sync.	
DVS	92	O	Display Vertical Sync.	
DCLK	93	O	Display Pixel Clock	
PD24	115	O	Red channel bit 0 (Odd)	Not used.
PD25	114	O	Red channel bit 1 (Odd)	Not used.
PD26	113	O	Red channel bit 2 (Odd)	Red channel bit 0 (Odd)
PD27	112	O	Red channel bit 3 (Odd)	Red channel bit 1 (Odd)
PD28	111	O	Red channel bit 4 (Odd)	Red channel bit 2 (Odd)
PD29	110	O	Red channel bit 5 (Odd)	Red channel bit 3 (Odd)
PD30	109	O	Red channel bit 6 (Odd)	Red channel bit 4 (Odd)
PD31	108	O	Red channel bit 7 (Odd)	Red channel bit 5 (Odd)
PD32	107	O	Green channel bit 0 (Odd)	Not used.

Pin Name	No	I/O	Description For 8-bit panels	For 6-bit panels
PD33	106	O	Green channel bit 1 (Odd)	Not used.
PD34	105	O	Green channel bit 2 (Odd)	Green channel bit 0 (Odd)
PD35	104	O	Green channel bit 3 (Odd)	Green channel bit 1 (Odd)
PD36	103	O	Green channel bit 4 (Odd)	Green channel bit 2 (Odd)
PD37	102	O	Green channel bit 5 (Odd)	Green channel bit 3 (Odd)
PD38	101	O	Green channel bit 6 (Odd)	Green channel bit 4 (Odd)
PD39	123	O	Green channel bit 7 (Odd)	Green channel bit 5 (Odd)
PD40	124	O	Blue channel bit 0 (Odd)	Not used.
PD41	125	O	Blue channel bit 1 (Odd)	Not used.
PD42	128	O	Blue channel bit 2 (Odd)	Blue channel bit 0 (Odd)
PD43	129	O	Blue channel bit 3 (Odd)	Blue channel bit 1 (Odd)
PD44	130	O	Blue channel bit 4 (Odd)	Blue channel bit 2 (Odd)
PD45	131	O	Blue channel bit 5 (Odd)	Blue channel bit 3 (Odd)
PD46	132	O	Blue channel bit 6 (Odd)	Blue channel bit 4 (Odd)
PD47	118	O	Blue channel bit 7 (Odd)	Blue channel bit 5 (Odd)

Note: In case of 24 Bit TTL Panels the RGB Odd Channel Outputs will not be used. In that case they can be made available for other purposes as Address & Data from On-Chip Micro or Digital Video Input Data.

Table 8: Parallel/Serial ROM Interface

Pin Name	No	I/O	Description
A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	95 96 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115	O	256K x8 PROM Address. These pins also have bootstrap functionality. For serial SPI ROM interface: - ROM_ADDR17 will be Serial Clock (ROM_SCLK) - ROM_ADDR16 will be Serial Data Output (ROM_SDO) For 512K X 8 PROM, Address Signal A18 is available thru Pin # 44 which is GPIO10.
D7 D6 D5 D4 D3 D2 D1 D0	132 131 130 129 128 125 124 123	IO	External PROM data input.
ROM_OEN	118	O	External PROM data Output Enable.
ROM_SDI/ ROM_WEN	97	O	External PROM data Write Enable (for In-System-Programming of FLASH) or Serial Data Input (SDI) for SPI ROM interface.
ROM_SCSN/ ROM_CSN	94	O	External PROM data Chip Select or Serial PROM Chip Select (ROM_SCSN) for SPI ROM interface.

Table 9: Digital Power and Ground

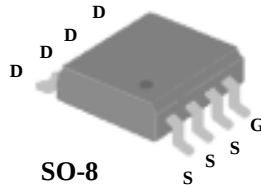
Pin Name	No	I/O	Description
RVDD_3.3	32 49 98 116 154	P	Ring VDD. Connect to digital 3.3V.
CVDD_1.8	18 28 39 45 84 119 126 133 143	P	Core VDD. Connect to digital 1.8V.
CRVSS	19 29 33 40 46 50 85 99 117 120 127 134 144 155	G	Chip ground for core and ring.

Table 10: JTAG Boundary Scan

Pin Name	No	I/O	Description
TCK	34	I	JTAG Boundary Scan TCK signal
TDO	55	O	JTAG Boundary Scan TDO signal
TDI	35	I	JTAG Boundary Scan TDI signal. Pad has internal 50K pull-up resistor.
TMS	36	I	JTAG Boundary Scan RST signal. Pad has internal 50K pull-up resistor.
TRST	37	I	JTAG Boundary Scan TMS signal. Pad has internal 50K pull-up resistor.



- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching

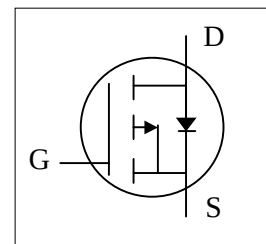


BV_{DSS}	-30V
$R_{DS(ON)}$	50m Ω
I_D	-5.3A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current ³	-5.3	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current ³	-4.7	A
I_{DM}	Pulsed Drain Current ¹	-20	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient ³ Max.	50	$^\circ\text{C}/\text{W}$

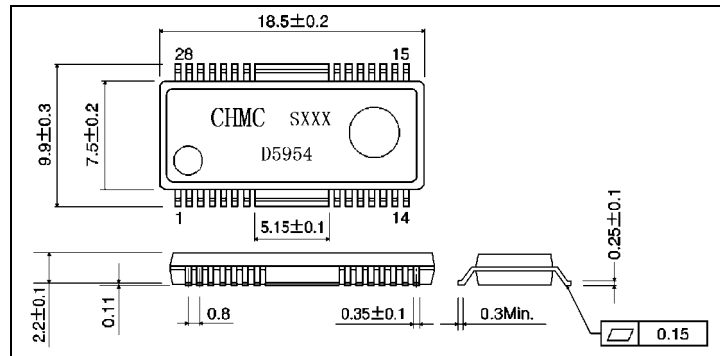


4 CHANNEL DRIVER MOTOR DRIVER D5954

DESCRIPTION

The D5954 is a 4 channel driver for optical disc motor driver. Dual channel current feedback type drivers are built in, in addition to dual channel motor drivers

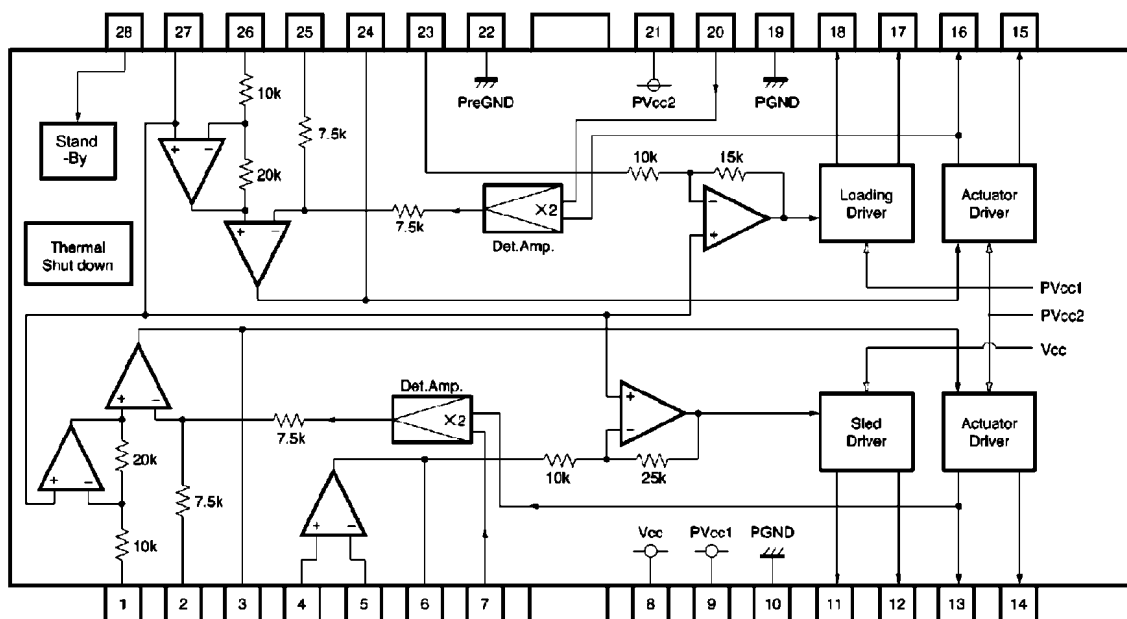
Outline Drawing



FEATURE

- Wide dynamic range. (4.0V (typ.) at PreVcc=12V,PVcc=5V,RL=8Ω)
- Separating Vcc into Pre+Power of sled motor, Power of loading motor and Power of actuator ,can make better power efficiency, by low supply voltage drive.
- Level shift circuit built in.
- Thermal-shut-down circuit built in
- Stand-by mode built in

BLOCK DIAGRAM



PIN DESCRIPTION

No	Symbol	Function	NO.	Symbol	Function
1	VINFC	Input for focus driver	15	VOTK+	Non inverting output for tracking
2	CECerr1	Connection with capacitor for error amplifier	16	VOTK-	Inverting output for tracking
3	CECerr2		17	OLD+	Non inverting output for loading
4	VINSL+	Non inverting input for OP-amp	18	VOLD-	Inverting output for loading
5	VINSL-	Inverting input for OP-amp	19	PGND	GND for power block
6	VOSL	Output of OP-amp	20	VNFTK	Feedback for tracking driver
7	VNFFC	Feedback for focus driver	21	PVcc2	Vcc for power block of actuator
8	Vcc	Vcc for pre-driver block and power block of sled	22	PreGND	GND for pre-drive block
9	PVcc1	Vcc for power block of loading	23	VINLD	Input for loading driver
10	PGND	GND for power block	24	CTKerr2	Connection with capacitor for error amplifier
11	VOSL-	Inverting output for sled	25	CTKerr1	
12	VOSL+	Non inverting output for sled	26	VINTK	Input for tracking driver
13	VOFC-	Inverting output for focus	27	BIAS	Input for reference voltage
14	VOFC+	Non inverting output for focus	28	STBY	Input for stand-by control

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply voltage	Vcc	13.5	V
Power dissipation	PD	1.7*	W
Operating temperature	Topr	-35~85	°C
Storage Temperature	Tstg	-40~150	°C

* On less than 3%(percentage occupied by copper foil), 70×70mm², t=1.6mm, glass epoxy mounting. Reduce power by 13.6mW for each degree above 25°C

Descriptions

- High current application
- Radio in class B push-pull operation

Feature

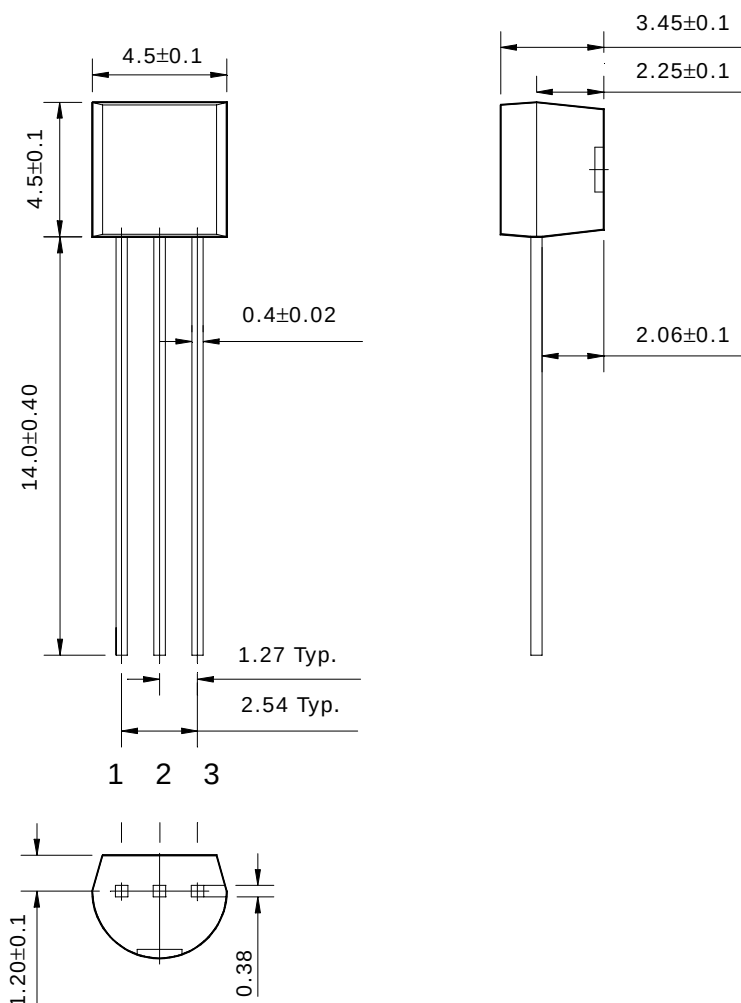
- Complementary pair with STS8550

Ordering Information

Type NO.	Marking	Package Code
STS8050	STS8050	TO-92

Outline Dimensions

unit : mm



PIN Connections

1. Emitter
2. Base
3. Collector

DVD SINGLE CHIP MPEG A/V PROCESSOR

1. GENERAL DESCRIPTION

SPHE8202D A/V decoder is a single-chip integrated DVD A/V decoder. It is designed to maximize system performance with minimum cost. It integrates DVD/CD controller, host processor, A/V decoding hardware, audio quality DAC and a 6-channel multi-format TV-encoder.

SPHE8202D supports DVD and CD physical formats. For logical formats it supports DVD-Video, Super Video CD, Video CD, CD-DA, OKO, and CD-ROM discs.

SPHE8202D performs real-time decoding and playback of

ISO/IEC 11172 MPEG1, 13818 MPEG2 sources. Besides MPEG A/V decoding, it supports Dolby Digital and MPEG/II Layer1/2, PCM, LPCM audio playback.

SPHE8202D also combines all the functions required for a high-performance progressive-scan DVD system. Built-in de-interlacing hardware allows high quality DVD playback. The embedded digital audio decoder is able to support key control and audio sound effects for Karaoke.

Development tools of SPHE8202D include complete compiler tools, programming guide and system application libraries.

Application utilizing the SPHE8202D is presented below:

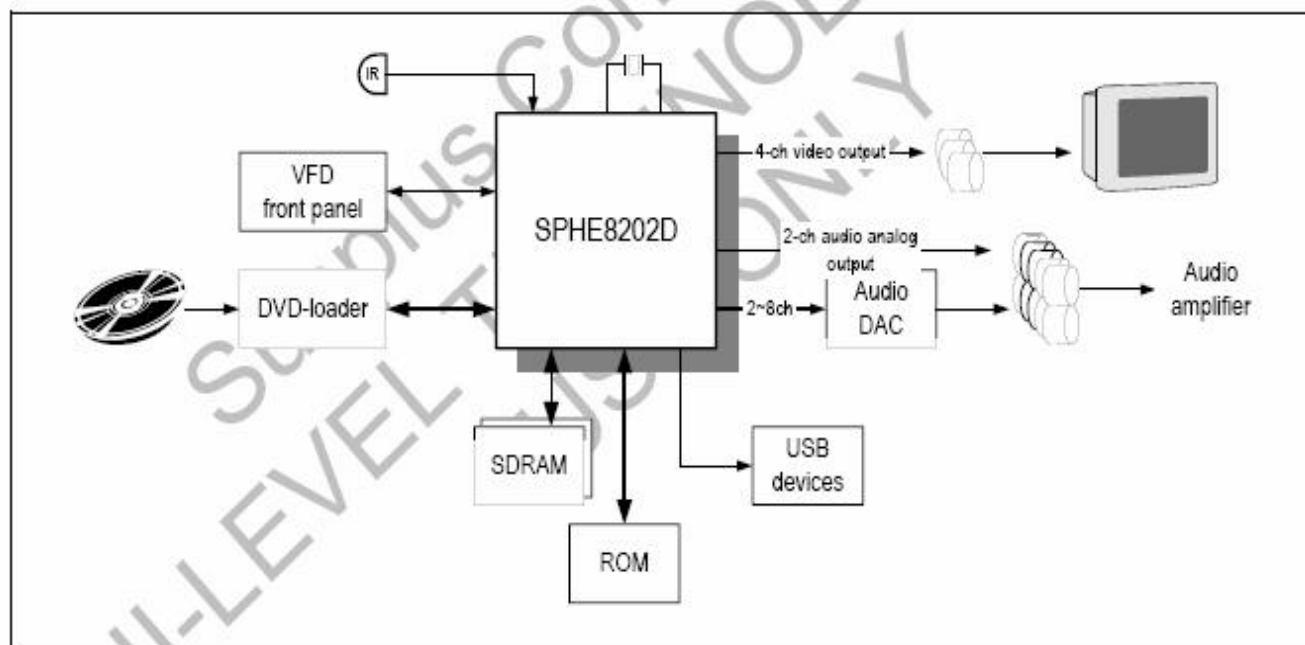


Figure 1-1 Sample SPHE8202D application

3.BLOCK DIAGRAM

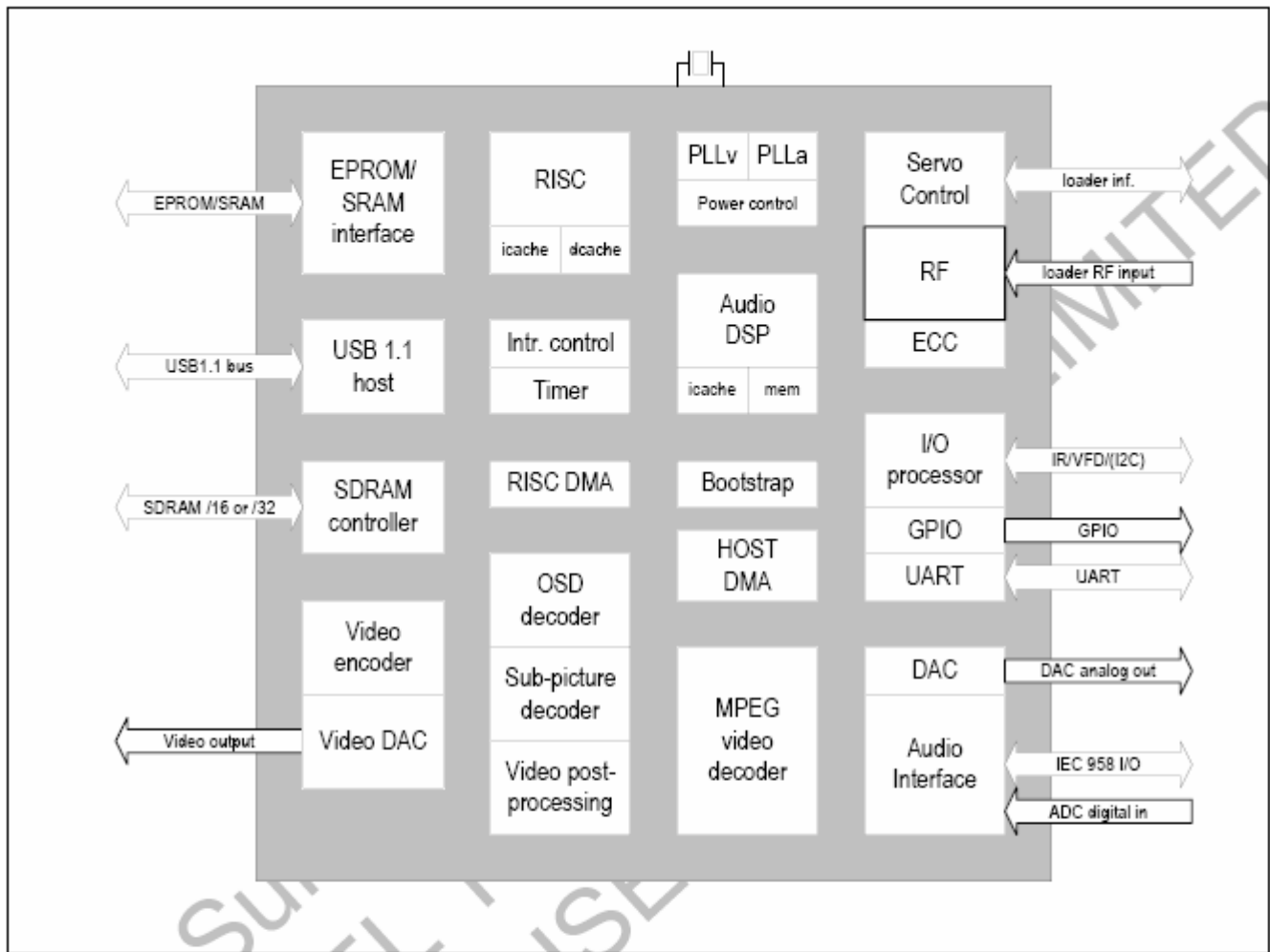


Figure 3-1 SPHE8202D block diagram

4. SIGNAL DESCRIPTION

4.1. Pin Map

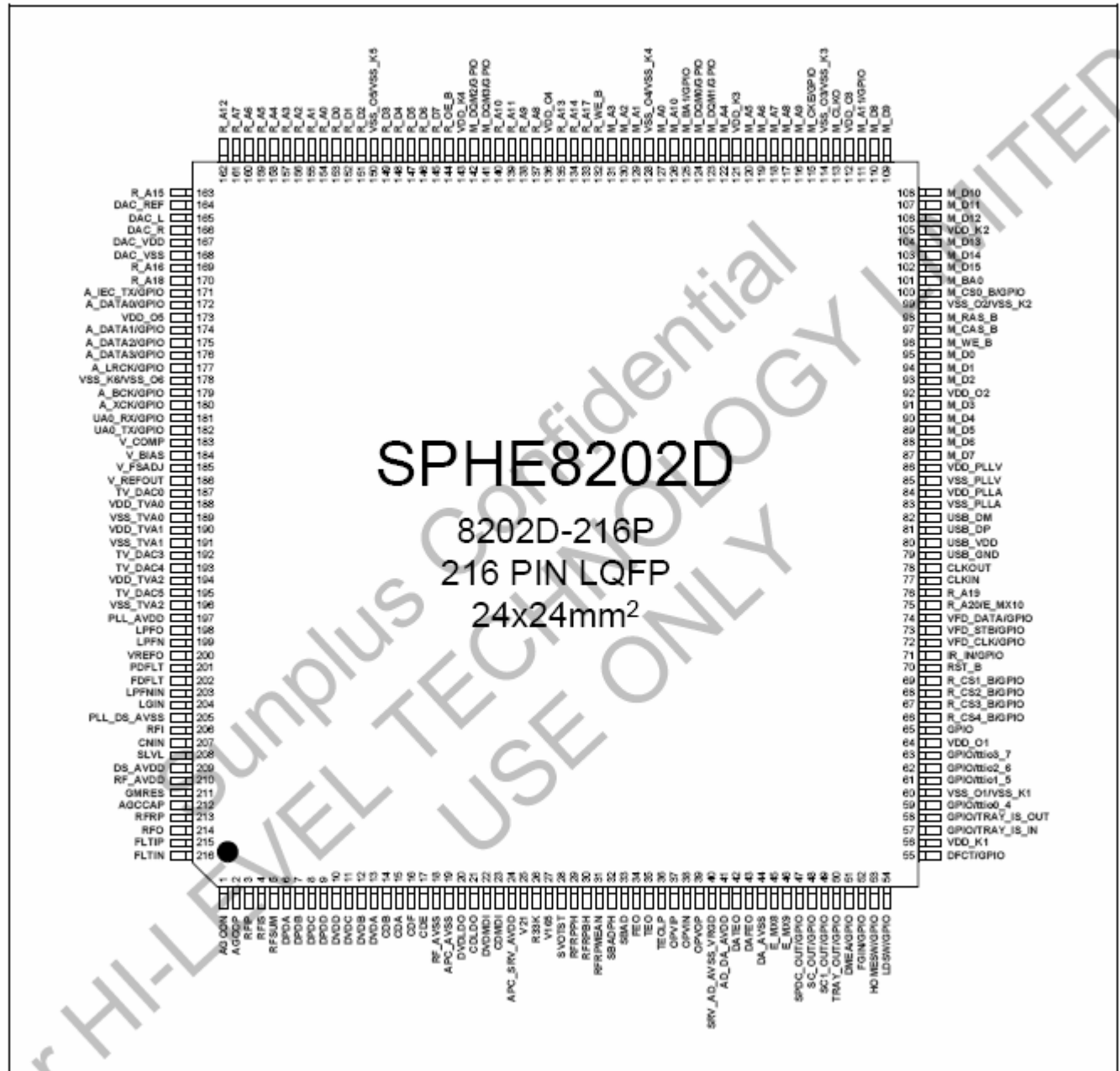


Figure 4-1 SPHE8202D pin



EN29LV800 **PRELIMINARY DRAFT**
8 Megabit (1024K x 8-bit / 512K x 16-bit) Flash Memory
Boot Sector Flash Memory, CMOS 3.0 Volt-only

FEATURES

- 2.7-3.6V $\pm$ 10%, single power supply operation
- Minimizes system level power requirements
- Manufactured on 0.28 μ m process technology
- High performance
 - Access times as fast as 55 ns
- Low power consumption (typical values at 5 MHz)
 - 7 mA typical active read current
 - 15 mA typical program/erase current
 - 1 μ A typical standby current (standard access time to active mode)
- Flexible Sector Architecture:
 - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
 - One 8 Kword, two 4 Kword, one 16 Kword and fifteen 32 Kword sectors (word mode)
 - Supports full chip erase
 - Individual sector erase supported
 - Sector protection:
 - Hardware locking of sectors to prevent program or erase operations within individual sectors
 - Additionally, temporary Sector Group Unprotect allows code changes in previously locked sectors.
- High performance program/erase speed
 - Byte program time: 10 μ s typical
 - Sector erase time: 200ms typical
 - Chip erase time: 3.5s typical
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Single Sector and Chip Erase
- Sector Unprotect Mode
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes:
 - Read and program another Sector during Erase Suspend Mode
- 0.25 μ m double-metal double-poly triple-well CMOS Flash Technology
- Latch-Up $\geq$ 200mA
- Low V_{cc} write inhibit $\leq$ 2.5V
- 100K endurance cycle
- 48-pin TSOP (Type 1)
- Commercial Temperature Range

GENERAL DESCRIPTION

The EN29LV800 is a 8-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 1,048,576 bytes or 524,288 words. Any byte can be programmed typically in 10 μ s. The EN29LV800 features 3.0V voltage read and write operation, with access times as fast as 55ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29LV800 has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.



CONNECTION DIAGRAMS

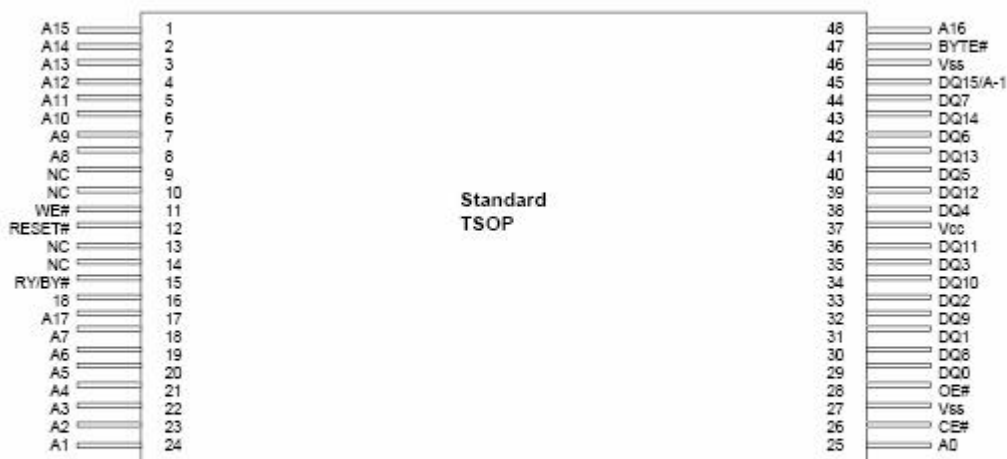
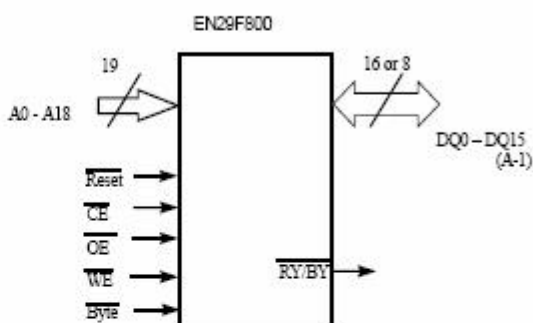


TABLE 1. PIN DESCRIPTION

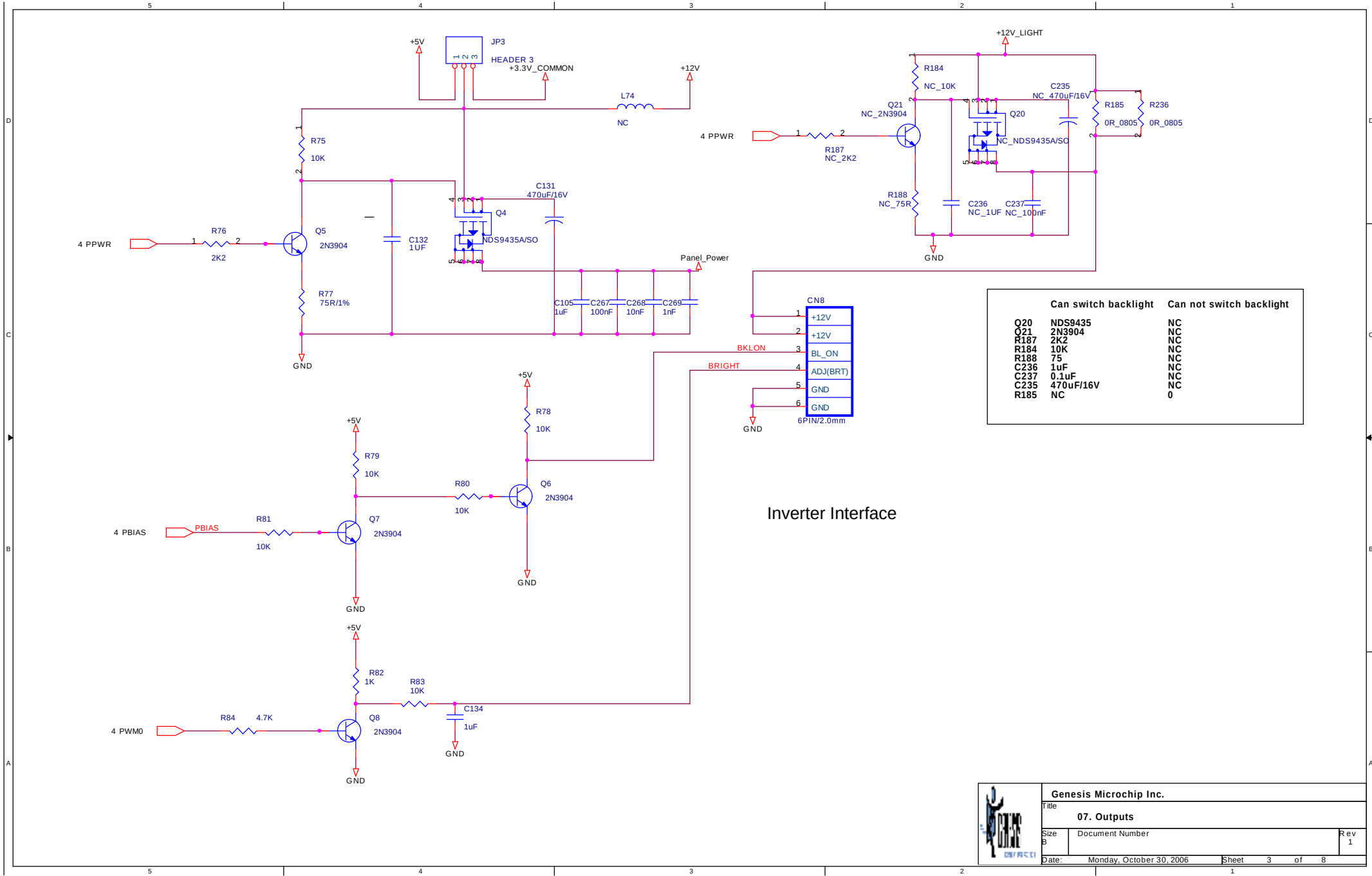
Pin Name	Function
A0-A19	Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE	Chip Enable
OE	Output Enable
Reset	Hardware Reset Pin
RY/BY	Ready/Busy Output
WE	Write Enable
Vcc	Supply Voltage (2.7-3.6V $\pm$ 10%)
Vss	Ground
NC	Internally connected pin

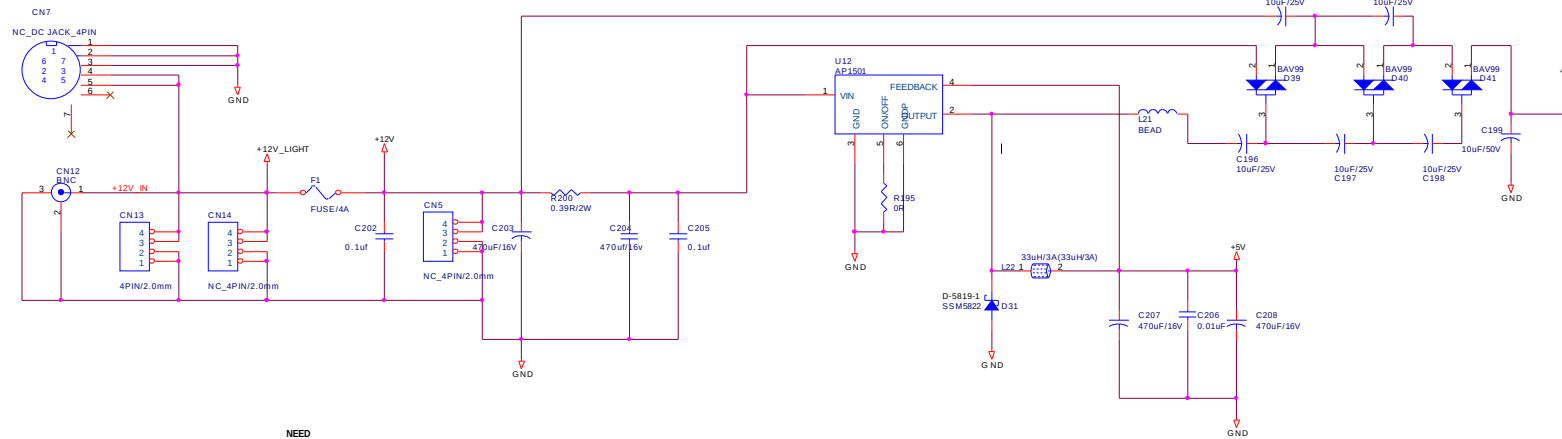
FIGURE 1. LOGIC DIAGRAM



Part4:

Detailed Circuit





TV Board Power

NEED
HEAT
SINK

U13
AIC1084-33CMTR, 5A Max
Adjust AB
TO-263

+5V

C209 100uF/16V

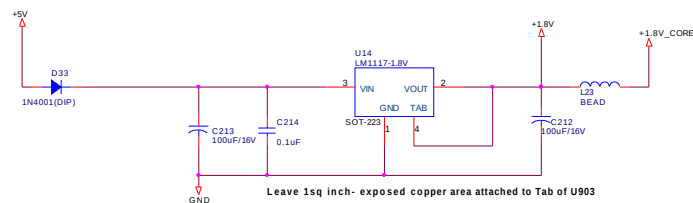
C210 0.1uF

+3.3V_COMMON

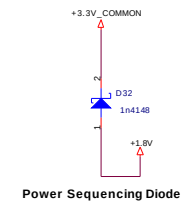
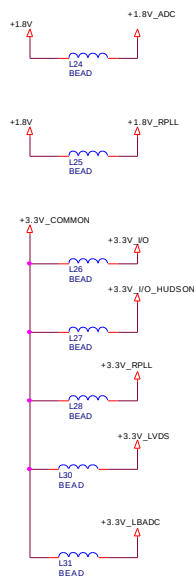
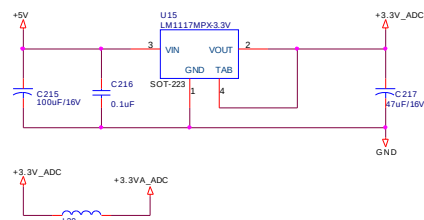
C211 100uF/16V

GND

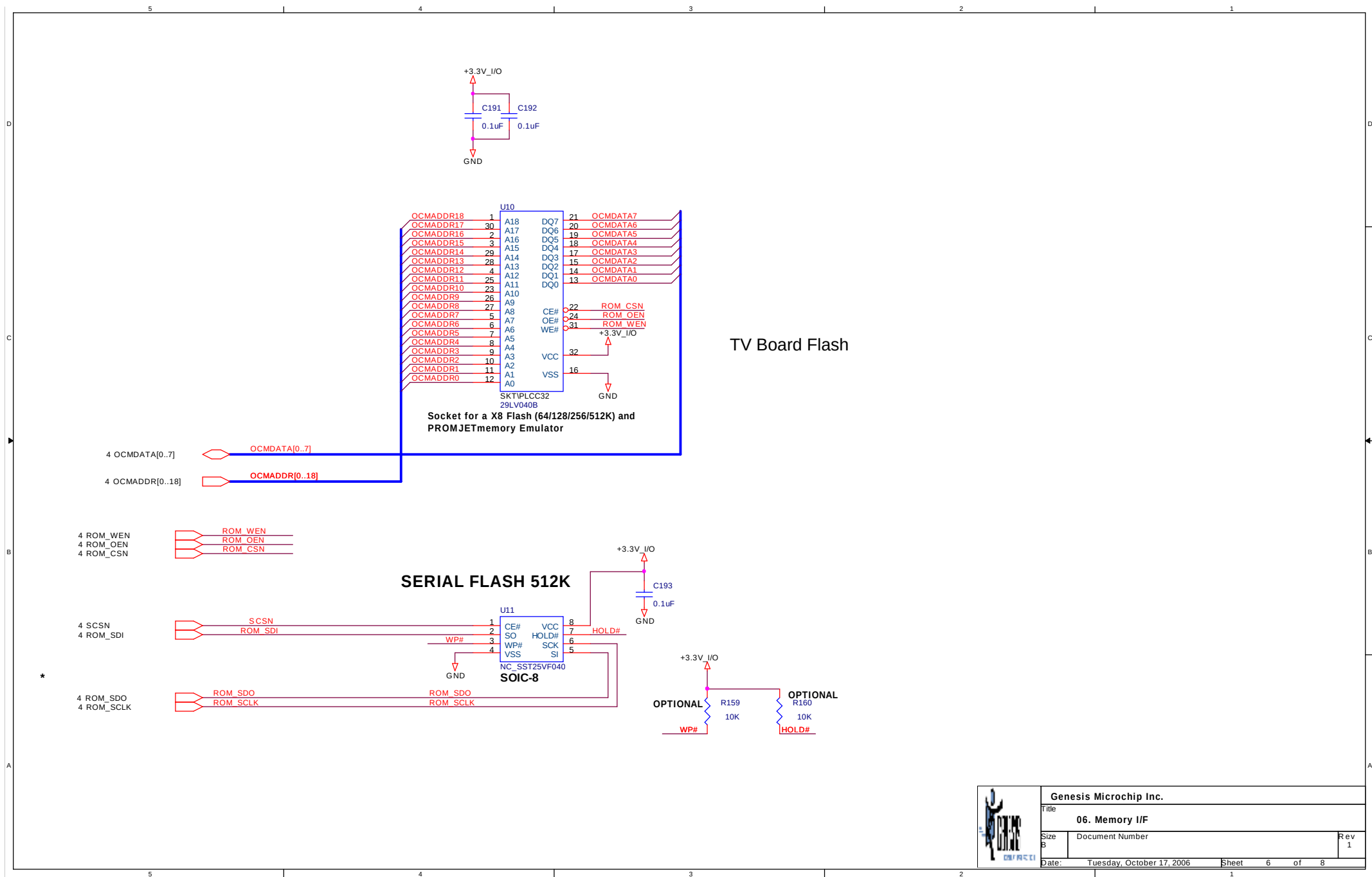
Leave 1sq inch- exposed copper area attached to Tab of U02
Leave room for heat sink

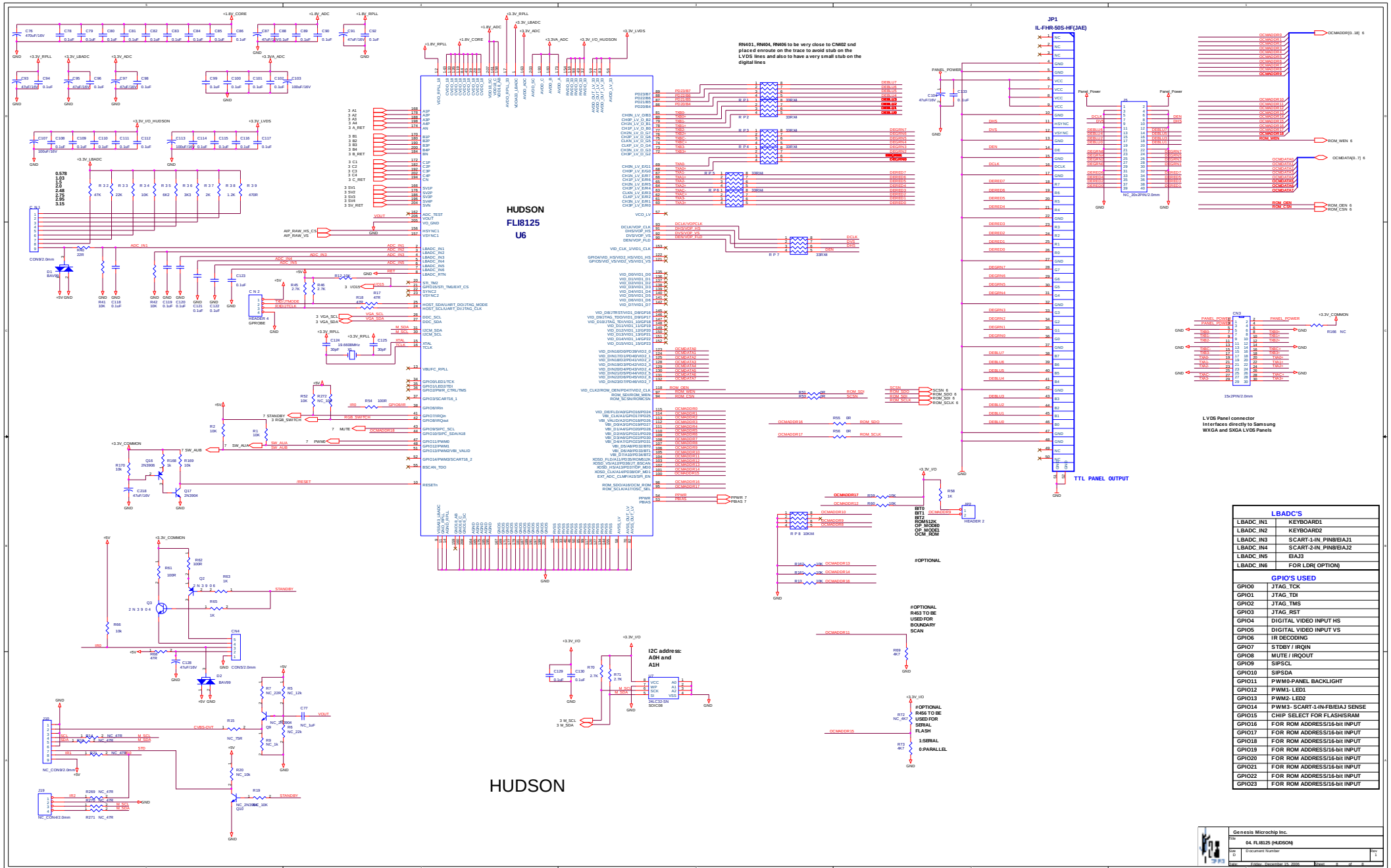


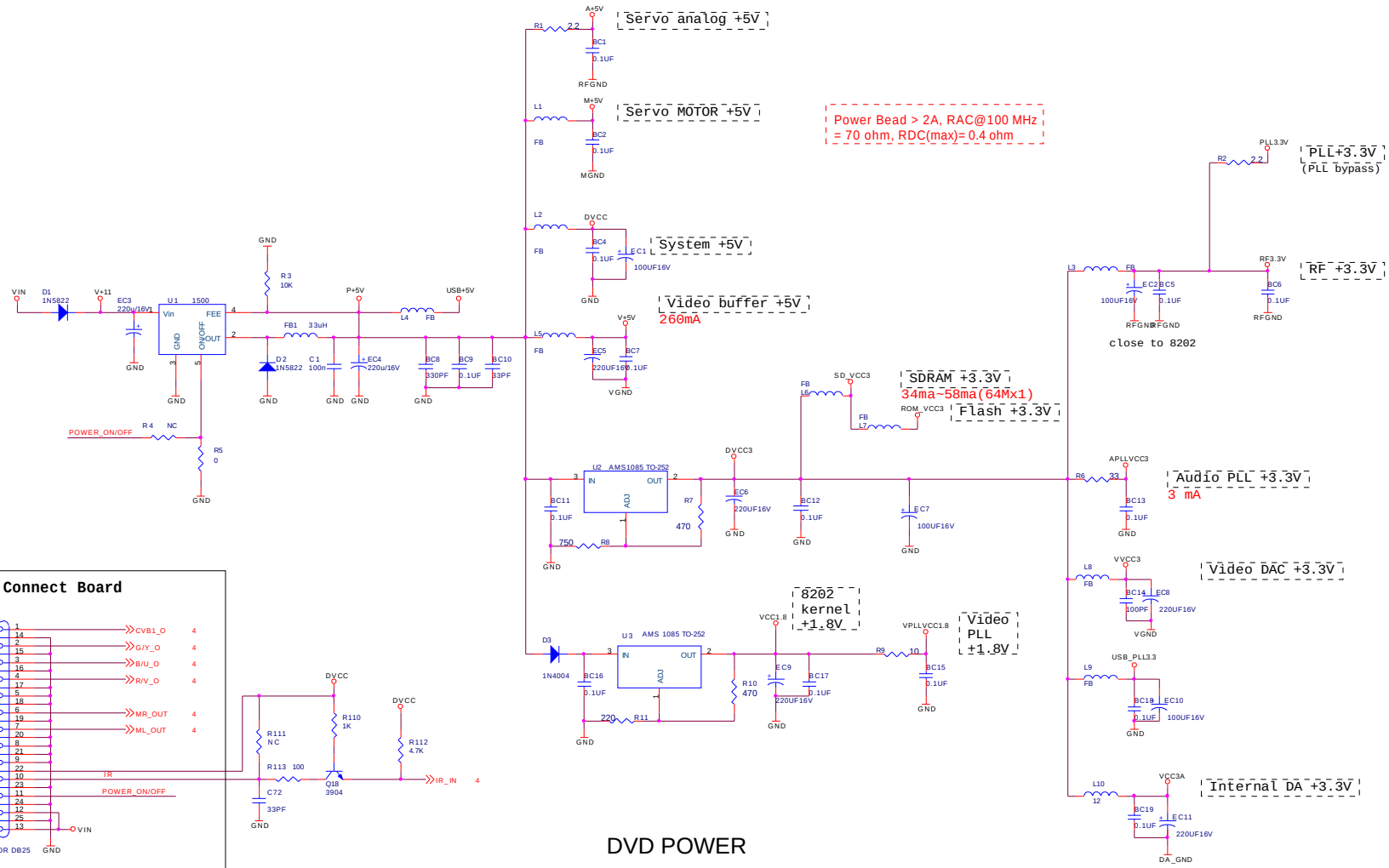
Leave 1sq inch- exposed copper area attached to Tab of U903



Power Sequencing Diode



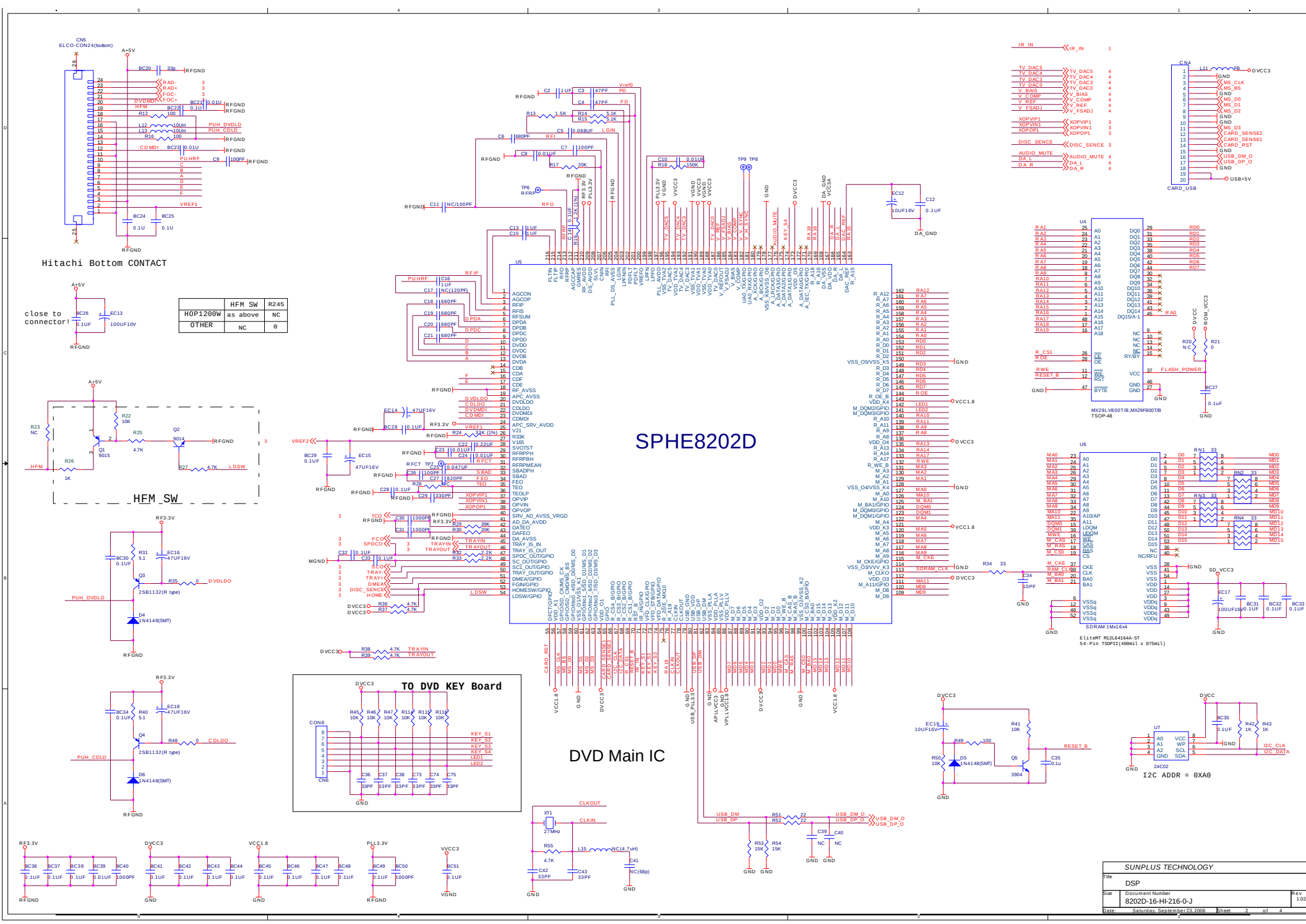




DVD POWER

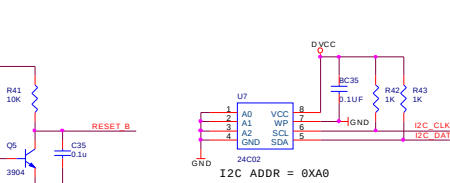
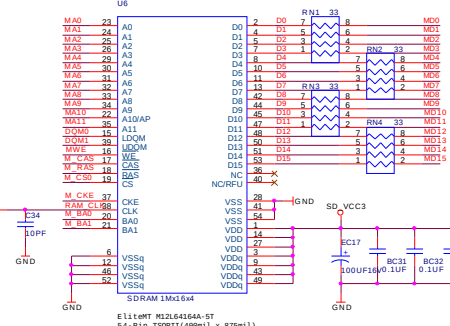
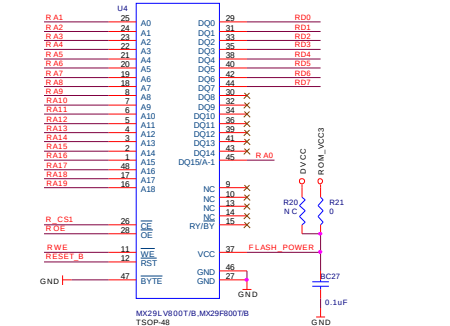
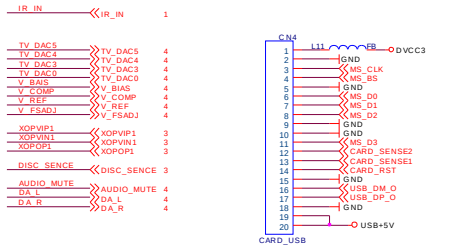
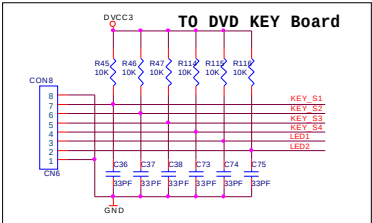


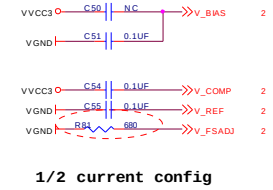
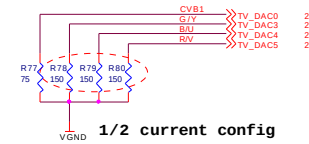
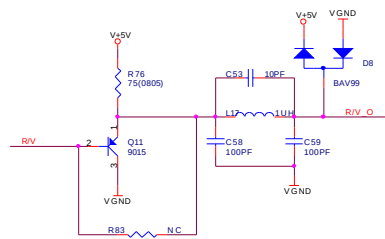
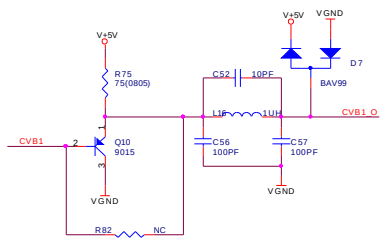
SUNPLUS TECHNOLOGY		
File	Power & Connector	
Size	Document Number	Rev
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Date	Saturday, September 23, 2006	Sheet 1 of 1



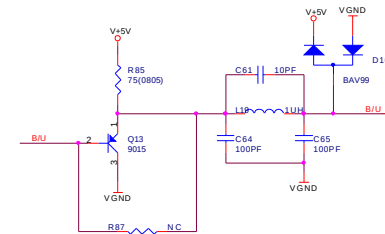
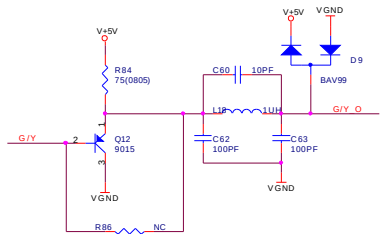
SPHE8202D

DVD Main IC

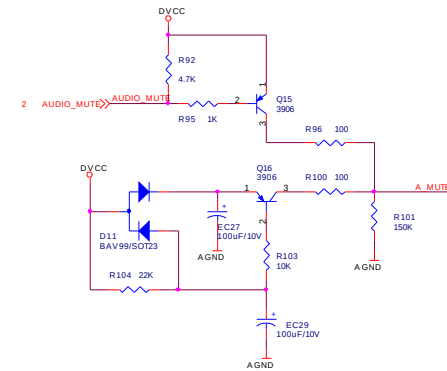
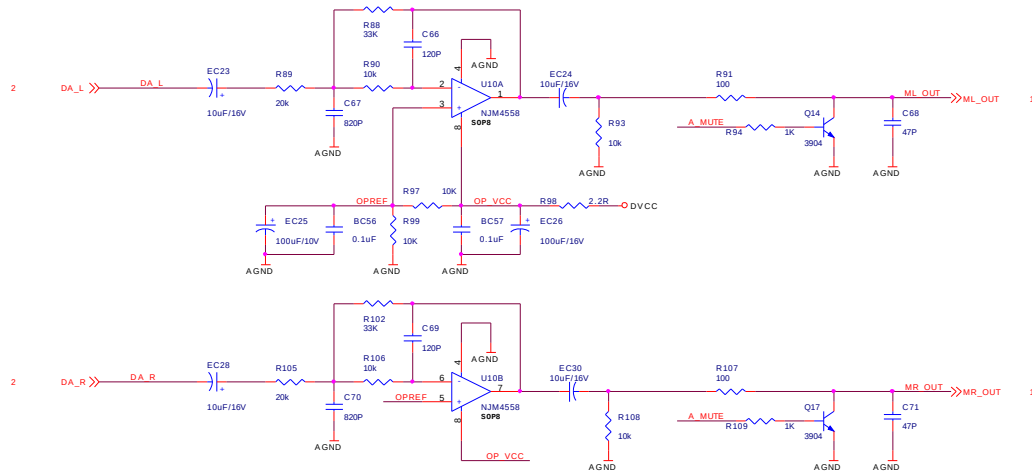




DVD Signal



VIDEO DAC	R118	R169	R268	R269	R270	R16	R17	R24
Full Current	390	0	0	0	0	75	75	75
Half Current	680	NC	NC	NC	NC	150	150	150



Part5:

Components List

TV Board BOM

序号	名称	规格型号	位号	用量	需求量	实发量
插座						
1	HEADER 2/2.54MM	2P插针式插针（连接器插针式2.54mm间距） 不带钩，立式	JP2	1		
2	HEADER 3/2.54MM	3P插针式插针（连接器插针式2.54mm间距） 不带钩，立式	JP3	1		
3	CON2/2.0MM	3P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	J4	1		
4	CON3/2.0MM	2P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	J3	1		
5	CON4/2.0MM	4P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	CN2,CN13	2		
6	CON5/2.0MM	5P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	CN4	1		
7	CON6/2.0MM	6P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	CN8	1		
8	CON9/2.0MM	9P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	CN1	1		
9	CON10/2.0MM	10P插针式插座（连接器插针式2.0mm间距） 不带钩，立式	J18	1		
10	F9370	声表	J16	1		
11	F3953M	声表	J17	1		
12	15X2PIN	15X2P插针式插针（连接器插针式2.0间距）	CN3	1		
13	IL-FHR-50S-HF	IL-FHR-50S-HF(JAE)	JP1	0		
14	SVIDEO JACK	Mini DIN JACK S端子	CN10	1		
15	DB15	DZ11A31-B8（15P-Dsub,30X15mm 卧式）	CN11	1		
16	BNC	DC+12V电源插座(巨大2.0mm)	CN12	1		
17	PHONE JACK	音频输入插座	J1	1		
18	SCP621U Y	黄	CN15	1		
19	SCP621U W	白	CN16	1		
20	SCP621U R	红	CN17	1		
21	component	AV端子(双层：绿.蓝.红+白.红)	CON5	1		
	晶振					
22	19.6608MT	19.6608MHz石英晶体振荡器(49S矮封装)	X1	1		
23	3.58MHZ	3.58MHz石英晶体振荡器(49S矮封装)	Y1	1		
24	4MHZ	4MHz石英晶体振荡器(49S矮封装)	Y2	1		
	二极管					
25	5.6V	稳压二极管 5.6Vz	D8,D21,D22	3		
26	5.1V	稳压二极管 5.1Vz	D14	1		
27	SSM5822	整流二极管60V/3A(肖特基)快恢复型,DII	D31	1		
28	1N4148	片状二极管LL4148（开关二极管）,DII	D32,D35,D36	3		
29	1N4001(DIP)	插件二极管1N4001	D33	1		
30	15V	稳压二极管 15Vz	D42	1		
31	17V/18V	稳压二极管 17Vz	D44	1		
	三极管					
32	BAV99	ESD片状三极管	D1,D2,D11,D15,D17,D18,D19,D20,D39,D40,D41	11		
33	2N3906	片状三极管,SOT23,PNP TR,VCE0=40V/IC=200mA,DII/AUK	Q2,Q16,Q34	3		
34	2N3904	片状三极管,SOT23,NPN TR,VCE0=40V/IC=200mA,DII/AUK	Q3,Q5,Q6,Q7,Q8,Q17,Q18,Q19,Q21,Q22,Q23,Q24,Q25,Q26,Q30,Q33	16		
	电解电容					
35	4.7uF/16V	DIP电解电容器(5X7) 16V ± 20%	2C25,2C26,2C27,2C28	4		
36	10uF/16V	DIP电解电容器(4X7) 16V ± 20%	2C15,2C21	2		
37	10uF/25V	DIP电解电容器(4X7) 16V ± 20%	C194,C195,C196,C197,C198	5		
38	10uF/50V	DIP电解电容器(4X7) 16V ± 20%	C246,C199	2		
39	22uF/16V	DIP电解电容器(4X7) 16V ± 20%	C34,2C24,2C29	3		
40	47uF/16V	DIP电解电容器(4X7) 16V ± 20%	2C2,2C8,C48,C87,C91,C93,C95,C97,C104,C128,C217,C218,C239,C240,C242,C258	16		
41	100uF/16V	DIP电解电容器(5X7) 16V ± 20%	C45,C53,C103,C107,C113,C209,C211,C212,C213,C215	10		
42	470uF/16V	DIP电解电容器（8X9）16V ± 20%	C46,C47,C76,C131,C203,C204,C207,C208,C222,C250	10		
	保险管					
43	FUSE/5A	熔断器5A轴向引线式(玻璃外壳)	F1	1		

	电感					
44	2.7uH	贴片0805	L5,L2	2		
45	22uH(DIP)	DIP色环電感器	L7,L3	2		
46	100uH(DIP)	立式固定電感器 for Tuner (4*6)	L4	1		
47	33uH/3A	环型立式固定電感器 33μH±20%	L22	1		
48	10UH	贴片式电感0805	L76	1		
49	L4.5M	DIP滤波器	T1	1		
	磁珠					
50	1K/100M	0805磁珠 1/16W ±5%	L77	1		
51	MG2012150YS	贴片式铁氧体磁珠0805 150Ω, 25%	L14,L16,L18,L32,L33,L34	6		
52	BEAD	贴片式铁氧体磁珠0805 150Ω, 25%	L21,L23,L24,L25,L26,L27,L28,L29,L30,L31	10		
	排阻					
53	33RX4	排状电阻器 KX0603 1/16W ±5%	RP1,RP2,RP3,RP4,RP5,RP6,RP7	7		
54	10K排阻	排状电阻器 KX0603 1/16W ±5%	RP8	1		
	贴片电阻					
55	0R	片状电阻器 KX0603 1/16W ±5%	R51,R53,R55,R56,R195,R233,R274,R275,R276	9		
56	0R 0805	片状电阻器 KX0805 1/16W ±5%	R236,R185	2		
57	0.39R/2W	插件电阻 2W	R200,R4	2		
58	3R	片状电阻器 KX0603 1/16W ±5%	R204,R205,R206,R207	4		
59	20R/1%	片状电阻器 KX0603 1/16W ±1%	R102,R105,R109,R112,R118,R121,R122,R130,R134,R139,R140,R145,R151,R215,R237,R238,R239	17		
60	22R	片状电阻器 KX0603 1/16W ±5%	R40	1		
61	47R	片状电阻器 KX0603 1/16W ±5%	R17,R18,R68,R214,R23,R22	6		
62	75R/ 1%	片状电阻器 KX0603 1/16W ±1%	R77,R103,R123,R125,R133,R136,R141,R152,R153,R154,R240,R241,R242	13		
63	75R	片状电阻器 KX0603 1/16W ±5%	R216	1		
64	100R	片状电阻器 KX0603 1/16W ±5%	R11,2R9,R54,R61,R62,R176,R180,R208,2R10,R211,R212,R226,R227	13		
65	150R	片状电阻器 KX0603 1/16W ±5%	R146,R150,R155,R156	4		
66	330	片状电阻器 KX0603 1/16W ±5%	R223	1		
67	470R	片状电阻器 KX0603 1/16W ±5%	R39	1		
68	1k	片状电阻器 KX0603 1/16W ±5%	R58,R63,R65,R82,R168,R173,R203,R213,R230,R231	10		
69	1.2K	片状电阻器 KX0603 1/16W ±5%	2R7,R38	2		
70	1.5K	片状电阻器 KX0603 1/16W ±5%	C249	1		
71	2K	片状电阻器 KX0603 1/16W ±5%	R37	1		
72	2.2K	片状电阻器 KX0603 1/16W ±5%	2R3,R225,R228,R76	4		
73	2.4K	片状电阻器 KX0603 1/16W ±5%	R24,R25,R26,R27,R28,R29	6		
74	2.7K	片状电阻器 KX0603 1/16W ±5%	R45,R46,R70,R71	4		
75	3K 0805	片状电阻器 KX0805 1/16W ±5%	R210,R209	2		
76	3K3	片状电阻器 KX0603 1/16W ±5%	R36	1		
77	3.9k	片状电阻器 KX0603 1/16W ±5%	R234	1		
78	4K7	片状电阻器 KX0603 1/16W ±5%	R69,R73,R157,R158,2R4,2R6,R84	7		
79	5.1K	片状电阻器 KX0603 1/16W ±5%	2R2	1		
80	5.6K	片状电阻器 KX0603 1/16W ±5%	R30,R31,R229	3		
81	6K2	片状电阻器 KX0603 1/16W ±5%	R35	1		
82	6.8K	片状电阻器 KX0603 1/16W ±5%	R175	1		
83	12K	片状电阻器 KX0603 1/16W ±5%	R222	1		
84	22K	片状电阻器 KX0603 1/16W ±5%	R232,R33	2		
85	47K	片状电阻器 KX0603 1/16W ±5%	R32,R177,R178	3		
86	10K	片状电阻器 KX0603 1/16W ±5%	R1,R2,R12,R13,2R1,2R5,2R8,R34,R41,R42,R52,R59,R60,R66,R75,R78,R79,R80,R81,R83,R143,R144,R159,R160,R161,R162,R169,R170,R174,R179,R190,R251,R252	33		
87	100K	片状电阻器 KX0603 1/16W ±5%	R3,R8,R191,R193,R224,R243,R244,R245,R246,R247,R248,R249,R250,R253,R254,R255,R256,R257,R258,R259,R260,R267,R268	23		
88	10M	片状电阻器 KX0603 1/16W ±5%	R194	1		
	贴片电容					
89	15pF	片状独石电容器CC41-0603 50V±20%	C270,C271,C272	3		
90	27PF	片状独石电容器CC41-0603 50V±5%	C35,C36,C37,C124,C125,C173,C179,C182,C1	9		

91	47pF	片状独石电容器CC41-0603 50V±20%	C190,C189	2		
92	100pF	片状独石电容器CC41-0603 50V±20%	C259	1		
93	150pF	片状独石电容器CC41-0603 50V±20%	2C5	1		
94	330pF	片状独石电容器CC41-0603 50V±20%	C147,C14	2		
95	390pF	片状独石电容器CC41-0603 50V±20%	C265	1		
96	680pF	片状独石电容器CC41-0603 50V±20%	C148,C15	2		
97	1000pF	片状独石电容器CC41-0603 50V±20%	C16,C269	2		
98	1200pF	片状独石电容器CC41-0603 50V±20%	2C6	1		
99	1.5nF	片状独石电容器CC41-0603 50V±20%	C255	1		
100	2.7nF	片状独石电容器CC41-0603 50V±20%	C63,C64,2C23	3		
101	10nF	片状独石电容器CC41-0603 50V±20%	C253,C261,C262,C263,C268,C206,2C11	7		
102	0.1uF/100nF	片状独石电容器CC41-0603 50V±20%	2C3,2C7,C43,C49,C57,C58,C59,C60,C65,C66,C78,C79,C80,C81,C82,C83,C84,C85,C86,C88,C89,C90,C92,C94,C96,C98,C99,C100,C101,C102,C108,C109,C110,C111,C112,C114,C115,C116,C117,C118,C119,C120,C121,C122,C123,C129,C130,C133,C136,C138,C139,C140,C141,C143,C146,C151,C152,C157,C164,C166,C167,C174,C178,C180,C181,C183,C184,C188,C191,C192,C193,C202,C205,C210,2C12,2C13,C214,C216,2C20,C227,C245,C248,C252,C256,C260,C267	86		
103	220nF	片状独石电容器CC41-0603 50V±20%	C257	1		
104	470nF	片状独石电容器CC41-0603 50V±20%	C254,C264	2		
105	1uF	片状独石电容器CC41-0603 50V±20%	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C38,C44,C52,C55,C56,C62,C68,C69,C105,C132,C134,2C18,2C19,C223,C229,C243,C244,C247,C251,C273,C274	31		
106	1uF_0805	片状独石电容器CC41-0805 50V±20%	2C4,2C9,2C10,2C22	4		
107	2.2uF_0805	片状独石电容器CC41-0805 50V±20%	2C14,2C16,2C17	3		
电路板						
108	PCB		HK-USA-DVD-YPBPR-L+R-V4.0	1		
芯片						
1	1a72700		U2	1		
2	SM9613		U3	1		
3	FLI8125	集成电路QFP208	U6	1		
4	24LC32-SN	半导体存储器S08(32K ROM), ST /Ceramate /SEC 厂家	U7	1		
5	TDA1517+散热片	DIP20	U8	1		
6	M24C02	半导体存储器S08(2K ROM),	U9	1		
7	29LV040B	SKT\PLCC32	U10	1		
8	AP1506-50K5LA AP1501-50K5LA	开关电源控制IC, 5A,T0263, Anachip /MATRIX 厂家	U12	1		
9	AP1084K-33LA	集成电路3.3V/5 A T0-263,Anachip /Gamma /ADD	U13	1		
10	1117-1.8V	功率集成电路SOT223(基准电压1.8V, 800mA),Anachip /MATRIX	U14	1		
11	LM1117MPX-3.3V	SOT223	U15	1		
12	CD4052	DIP16-SOP	U17	1		
13	TAD9886/9885	DIP24-SOP-1.27	U19	1		
14	78D09	SMD-T0-252-4	U25	1		
15	APM9435A	片状场效应晶体管S08, P沟道SW	Q4	1		
16	AP2301	SOT-23	Q22	1		
17	TUNER:	高频头 UVL7605VMW	J8	1		

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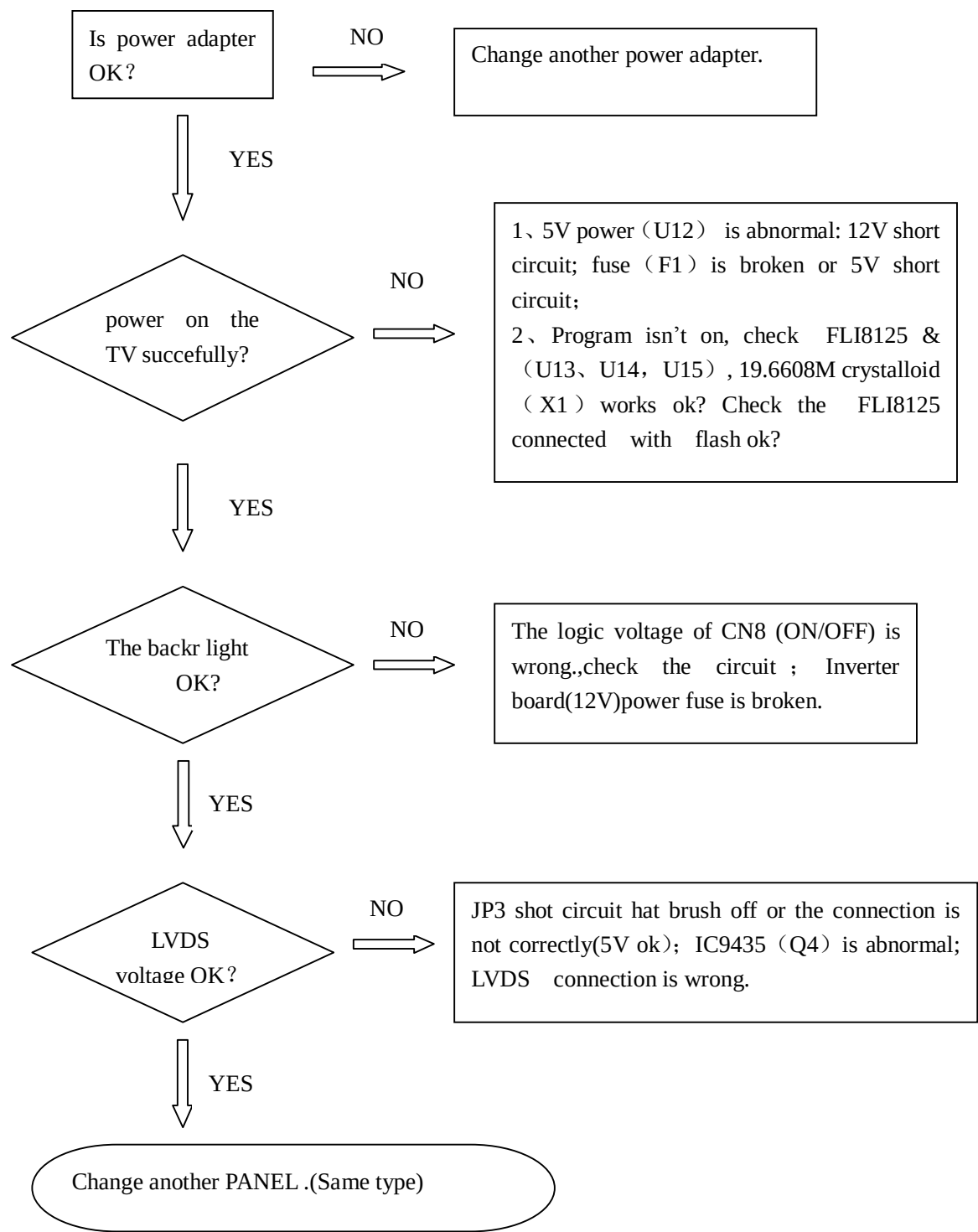
序号	名称	规格型号	位号	用量	需求量	实发量
贴片电容						
1	100NF	片状独石电容器CC41-0603 50V±20%	BC1,BC2,BC4,BC5,BC6,BC7,BC9,BC11,C12,BC12,BC13,C14,BC15,BC16,BC17,BC18,BC19,BC26,BC27,C28,BC28,BC29,BC30,BC31,C32,BC32,C33,BC33,BC34,BC35,BC36,BC37,BC38,BC41,BC42,BC43,BC44,BC45,BC46,BC47,BC48,BC49,C51,BC51,BC52,BC53,C54,BC54,C55,BC55,BC56,BC57,BC22,BC24,BC25,C35,C1	57		
2	330PF	片状独石电容器CC41-0603 50V±20%	C29,BC8, C44,C45	4		
3	33PF	片状独石电容器CC41-0603 50V±20%	BC10,C36,C37,C38,C42,C43,C72, BC20	8		
4	100PF	片状独石电容器CC41-0603 50V±20%	C7,C9,BC14,C26,C56,C57,C58,C59,C62,C63,C64,C65	12		
5	10nF	片状独石电容器CC41-0603 50V±20%	BC21,BC23, C8,C10,C23,C24,BC39	7		
6	1000PF	片状独石电容器CC41-0603 50V±20%	C30,C31,BC40,BC50	4		
7	1UF	片状独石电容器CC41-0603 50V±20%	C2,C13,C15,C16,BC3	5		
8	47PF	片状独石电容器CC41-0603 50V±20%	C4,C3, C68,C71	4		
9	68nF	片状独石电容器CC41-0603 50V±20%	C5	1		
10	680PF	片状独石电容器CC41-0603 50V±20%	C6,C18,C19,C20,C21	5		
11	220nF	片状独石电容器CC41-0603 50V±20%	C22	1		
12	47nF	片状独石电容器CC41-0603 50V±20%	C25	1		
13	820PF	片状独石电容器CC41-0603 50V±20%	C27 ,C70,C67	3		
14	10PF	片状独石电容器CC41-0603 50V±20%	C34,C52,C53,C60,C61	5		
15	4700PF	片状独石电容器CC41-0603 50V±20%	C47,C46	2		
16	390PF	片状独石电容器CC41-0603 50V±20%	C48,C49	2		
17	120P	片状独石电容器CC41-0603 50V±20%	C69,C66	2		
二极管						
18	IN5820	DIP整流二极管60V/3A(肖特基)快恢复型,DII	D2,	1		
19	1N4004	DIP二极管 (开关二极管),DII	D3 ,D1	2		
20	1N4148	片状二极管LL4148 (开关二极管),DII	D4,D5,D6	3		
21	BAV99	ESD片状二极管	D7,D8,D9,D10, D11	5		
电解电容						
22	100UF16V	DIP电解电容器(6.3X5) 16V ± 20%	,EC6,EC8,EC9,EC11,EC22,EC13,	6		
23	100UF16V	DIP电解电容器(5X11) 16V ± 20%	EC1,EC26,EC25,EC27,EC29,EC21,EC7,EC10,EC17,	9		
24	10UF16V	DIP电解电容器(4X5) 16V ± 20%	EC12,EC19, EC23,EC24,EC28,EC30	6		
25	47UF16V	DIP电解电容器(5×5) 16V ± 20%	EC15,EC16,EC18 ,	3		
26	47UF10V	SMT钽电容 10V ± 20%	EC14	1		
27	4.7UF16V	DIP电解电容器(4X5) 16V ± 20%	EC20	1		
28	220u/16V	DIP电解电容器(6.3X7) 16V ± 20%	EC3,EC4 ,EC5	3		
29	220UF16V	DIP电解电容器(8X5) 16V ± 20%	EC2	1		
30	470UF16V	DIP电解电容器(8X7) 16V ± 20%	EC32	1		
电感						
31	33uH	环型立式固定电感器 33 μ H±20% 3A	FB1	1		
32	10UH	SMT0805贴片式电感器 for Tuner	L12,L13	2		
33	1UH	SMT0805贴片式电感器 for Tuner	L16,L17,L18,L19	4		
磁珠						
34	FB 75Ω	0805贴片式磁珠	L1,L2,L3,L4,L5,L6,L7,L8,L9, L10,L11	11		
三极管						
35	9015	三极管SOT23	Q1,Q10,Q11,Q12,Q13	5		
36	9014	三极管SOT23	Q2	1		
37	2SB1132	BAR	Q3,Q4	2		
38	3904	三极管SOT23	Q5,Q18	2		
39	3906	三极管SOT23	Q16,Q15	2		
40	S8550D	三极管S0-92	Q7,Q6	2		
41	S8050D	三极管S0-92	Q8,Q9	2		
排阻						
42	33Ω	片状电阻器 KX0603 1/16W ±5%	RN1,RN2,RN3,RN4,	4		
贴片电阻						
43	0Ω	片状电阻器 KX0603 1/16W ±5%	R4,R21,R35,R48 ,R11,R8	6		

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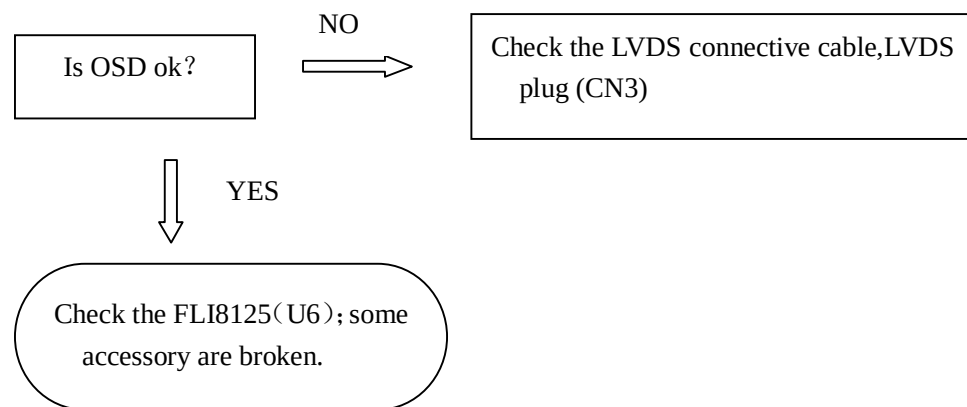
序号	名称	规格型号	位号	用量	需求量	实发量
44	1Ω	片状电阻器 KX0603 1/16W ±5%	R56,R57,R59,R60,R63	5		
45	2.2Ω	片状电阻器 KX0603 1/16W ±5%	R1,R2, R98	3		
46	5.1Ω	片状电阻器 KX0603 1/16W ±5%	R40,R31	2		
47	10Ω	片状电阻器 KX0603 1/16W ±5%	R9	1		
48	22Ω	片状电阻器 KX0603 1/16W ±5%	R51,R52	2		
49	33Ω	片状电阻器 KX0603 1/16W ±5%	R6,R34	2		
50	75Ω 0805	片状电阻器 KX0805 1/16W ±5%	R75,R76,R84,R85	4		
51	75Ω	片状电阻器 KX0603 1/16W ±5%	R77,	1		
52	100Ω	片状电阻器 KX0603 1/16W ±5%	R12,R16,R49,R91,R96,R100,R107,R113	8		
53	150Ω	片状电阻器 KX0603 1/16W ±5%	R78,R79,R80	3		
54	220Ω	片状电阻器 KX0603 1/16W ±5%	R69,R70	2		
55	680Ω	片状电阻器 KX0603 1/16W ±5%	R72,R71, R81	3		
56	1KΩ	片状电阻器 KX0603 1/16W ±5%	R26,R42,R43,R73,R74,,R95,R110	7		
57	1.2KΩ (1%)	片状电阻器 KX0603 1/16W ±1%	R19	1		
58	2.2KΩ	片状电阻器 KX0603 1/16W ±5%	R33,R32	2		
59	1.5KΩ	片状电阻器 KX0603 1/16W ±5%	R13	1		
60	4.7KΩ	片状电阻器 KX0603 1/16W ±5%	R25,R27,R36,R37,R38,R39,R55,R92,R112	9		
61	5.1KΩ	片状电阻器 KX0603 1/16W ±5%	R15,R14	2		
62	6.2KΩ	片状电阻器 KX0603 1/16W ±5%	R68	1		
63	10KΩ	片状电阻器 KX0603 1/16W ±5%	R3,R22,R41,R45,R46,R47,R50,R67,R90,R93, R97,R99,R103,R106,R108,R114,R115,R116	18		
64	15KΩ	片状电阻器 KX0603 1/16W ±5%	R53,R54	2		
65	20KΩ	片状电阻器 KX0603 1/16W ±5%	R17,R30,R89,R105	4		
66	22KΩ	片状电阻器 KX0603 1/16W ±5%	R58,R61,R104	3		
67	33KΩ (1%)	片状电阻器 KX0603 1/16W ±1%	R24	1		
68	33KΩ	片状电阻器 KX0603 1/16W ±5%	R88,R102	2		
69	39KΩ	片状电阻器 KX0603 1/16W ±5%	R29	1		
70	150KΩ	片状电阻器 KX0603 1/16W ±5%	R18,R64,R65,R101	4		
71	470KΩ	片状电阻器 KX0603 1/16W ±5%	R62,R66	2		
IC类						
72	1500-50		U1	1		
73	LM1117-3.3		U2	1		
74	LM1117-1.8		U3	1		
75	EN29LV800BA		U4	1		
76	SPHE8202D		U5	1		
77	1Mx16x4	HY57V641620ETP	U6	1		
78	24C02		U7	1		
79	D5954		U8	1		
80	LM7808		U9	1		
81	NJM4558		U10	1		
晶振						
82	27MHz	石英晶体振荡器(矮封装)20pF	XT1	1		
插座						
83	CONNECTOR DB25	卧式 公座	CN1	1		
84	20PIN-1.0mm	DIP插针式插座(1.0间距)	CN4	1		
85	24PIN-0.5mm	SMT卧式贴片插座0.5间距)	CN5(塑胶缺口和丝印反向)	1		
86	8P-2.0mm	DIP立式插针式插座(2.0间距)	CN6	1		
87	12PIN-1.0mm	SMT卧式贴片插座(1.0间距)	CN7	1		
电路板						
88	PCB	MPEG_BOARD V2.0		1		

FLI8125 TV block DEBUG INSTRUCTION

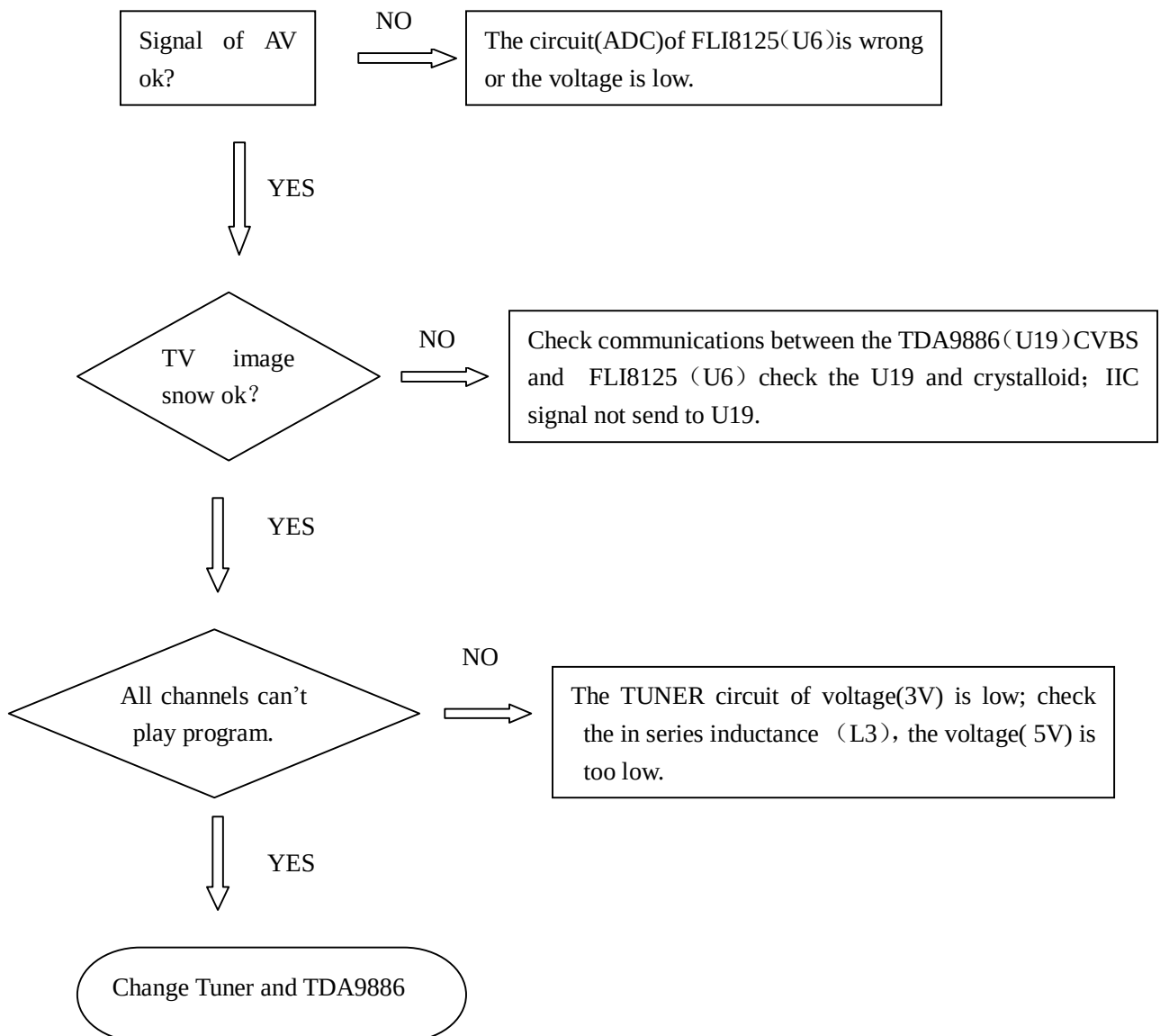
1.BALCK SCREEN



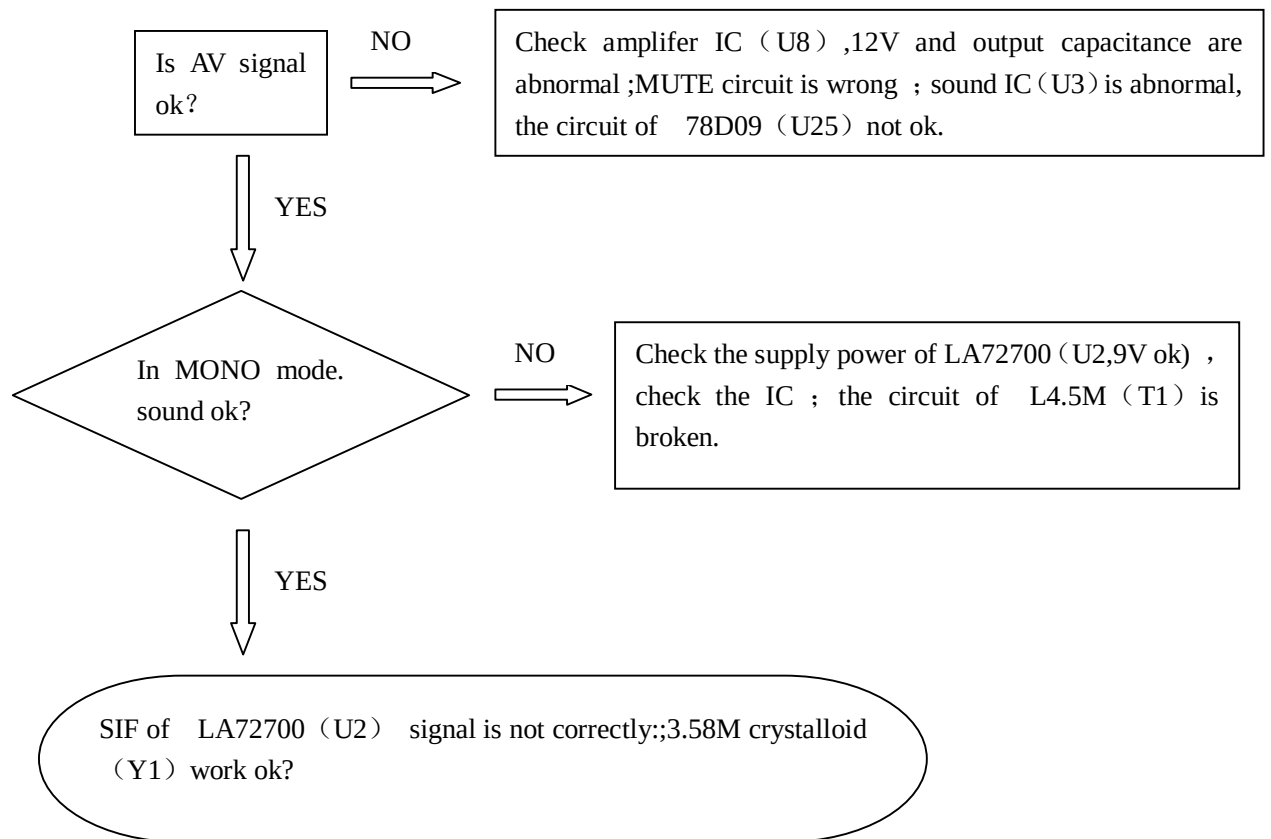
2.ABNORMAL PICTURE



3.NO TV SIGNAL

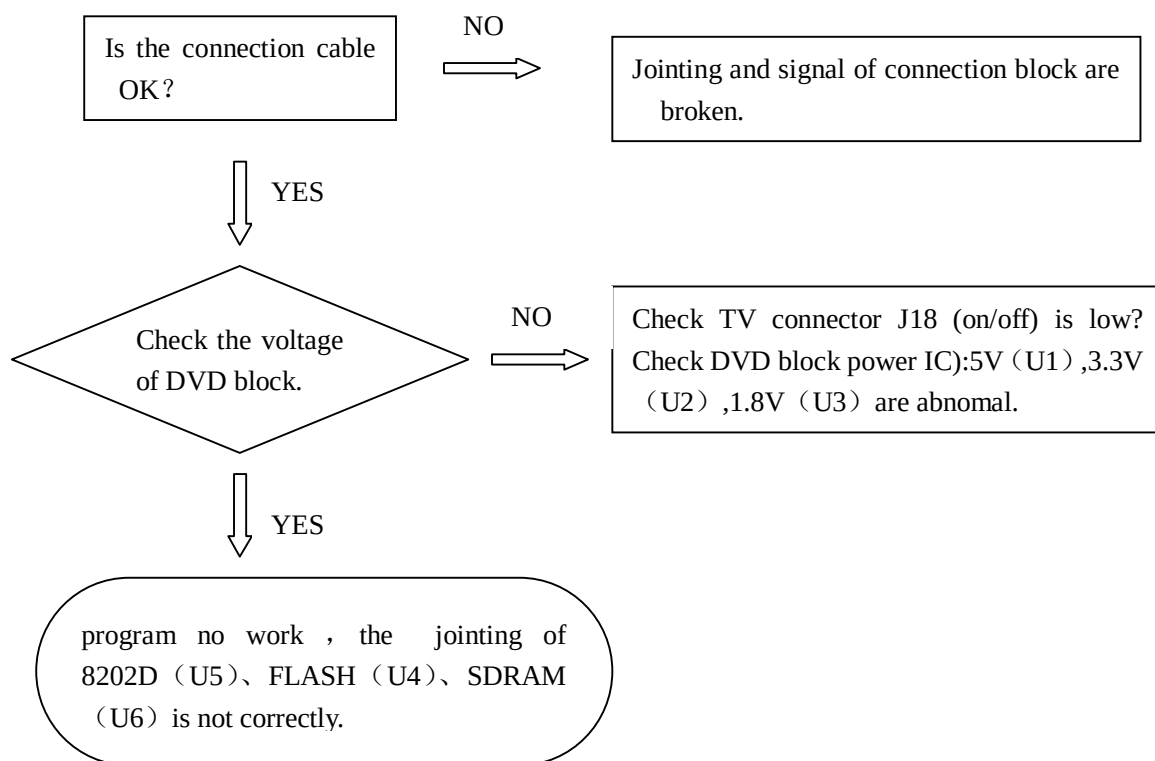


4.TV NO SOUND

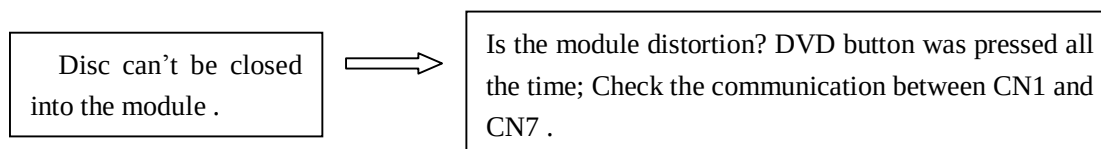


DVD BLOCK DEBUG INSTRUCTION

1.DVD NO PICTURE



2. DVD MODULE CAN'T CLOSE



3. DISC CAN'T BE READ

